Raytheon

RF Vacuum Microelectronics

FINAL REPORT

Contract No. MDA972-91-C-0032
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The result of the 18 month research and development project on high frequency Field Emission Array (FEA) cathodes is presented. Details of the process development and test procedures are discussed. The results relative to the program goals are presented. Finally, suggestions for future work in the 12 month option portion of the project are presented.

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1.0 INTRODUCTION

Vacuum Microelectronics technology is an attempt to combine the best features of low cost solid state fabrication techniques and vacuum tube electronics. One goal is the development of cathodes that can be modulated at the carrier (not a modulation) frequency. This concept has worked well at UHF frequencies with gridded cathodes to reduce tube size and increase efficiency. To push this concept up into the microwave frequencies requires a new technology. This is because the small grid spacings required can not be manufactured with conventional tube technology. The new technology is micron-sized gated field emission cathode arrays. The program goals were to fabricate triode structures that met the following criteria:

1. $F_t = g_m/2\pi C_g > 1$ GHz
2. $V_g < 250$ volts
3. $J > 5$ A/cm^2
4. $I > 5$ mA

The nomenclature for the triode's ports is a mixture of solid state FET and tube terms. The electrons start from the field emitter cathode (source), are modulated by the gate (grid), and are collected by the anode (drain).

The first criteria F_t is the ratio of the small signal transconductance g_m to the gate capacitance C_g. This a measure of the maximum operating frequency of the triode. The second criteria V_g is the gate voltage required to obtain the g_m in the first term and J and I in the following terms. J is the current density and I is the total current at the operating point. The operating life had to be at least one hour. The anode voltage and duty cycle were not specified.

Section 2.0 presents the processes developed to fabricate the cathodes. Two types of cathodes; tip and circular edge are described. Section 3.0 presents the results from two test approaches; a planar (MMIC like) triode and a cylindrical (tube like) triode. Section 4.0 is a detailed investigation into the gate capacitance issue. Section 5.0 concludes with suggestions for future work.

2.0 PROCESS DEVELOPMENT

2.1 Overview

Two emitter structures were fabricated; tip and circular edge. The process development was started for another application under Raytheon Company IR&D funding. The processes were extended and improved under this contract. Standard semiconductor processing is used where possible. Stepper photolithography was used for all the masking steps. The two processing steps that required extensive work over conventional techniques were in the Reactive Ion Etching (RIE) of the metals and the thick metal evaporation steps.

All the emitter devices use molybdenum for all metal layers. Molybdenum may not be the best choice because there are materials with smoother surfaces and/or lower work functions that may give higher emission currents for a given gate voltage. Also, there are some processing difficulties with molybdenum, such as its relatively poor adherence to the silicon dioxide dielectric layers. However, the silicon dioxide to molybdenum etch rate ratio is very high which makes for a relatively easy stack etch.

2.2 Tip Emitter

Our baseline approach is to form a conventional micron sized tip Field Emission Array (FEA) cathodes using a metal insulator stack on a metal layer on which cone-type field emitters are formed. The metal layers are 3,000 angstroms of molybdenum and the dielectric layers are 8,000 to 10,000 angstroms of low temperature CVD oxide (LTO). The tips are made by evaporation into micron sized holes spaced on 6 micron to as small as 2.5 micron centers (see Figure 2-1). The process is illustrated in Figure 2-2, Steps I through X.

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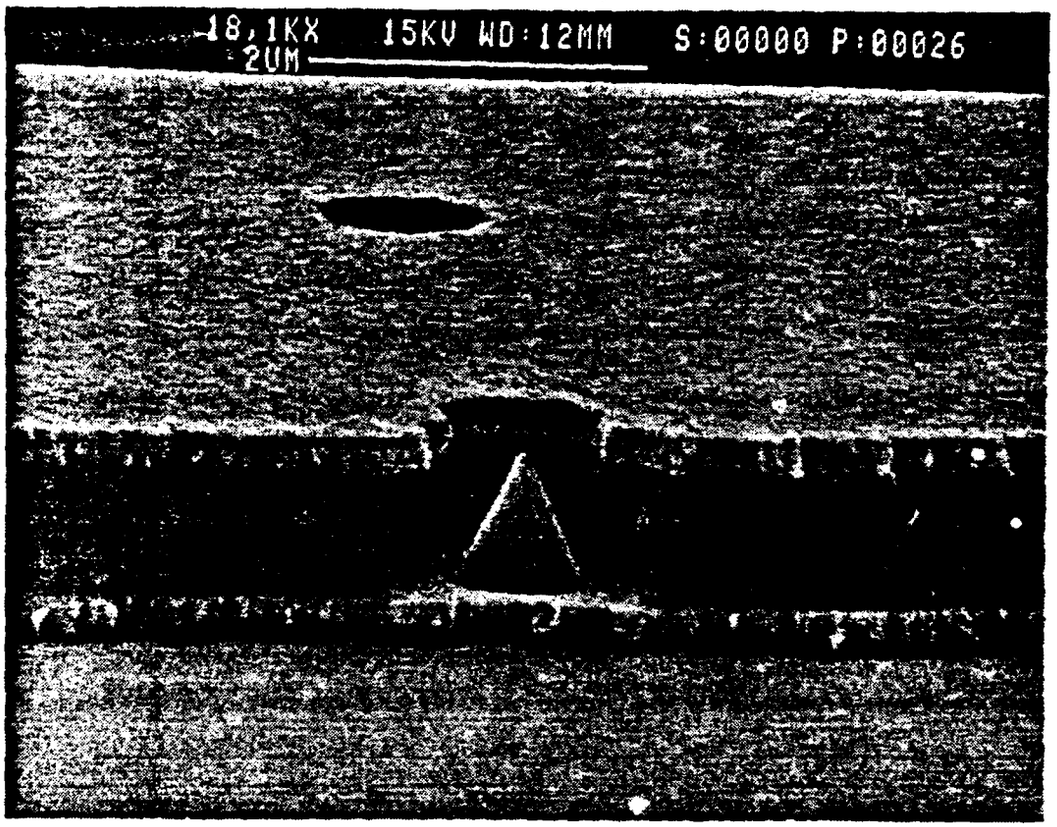


Figure 2-1. A Portion of a Fabricated Tip Emitter Array Cathode.

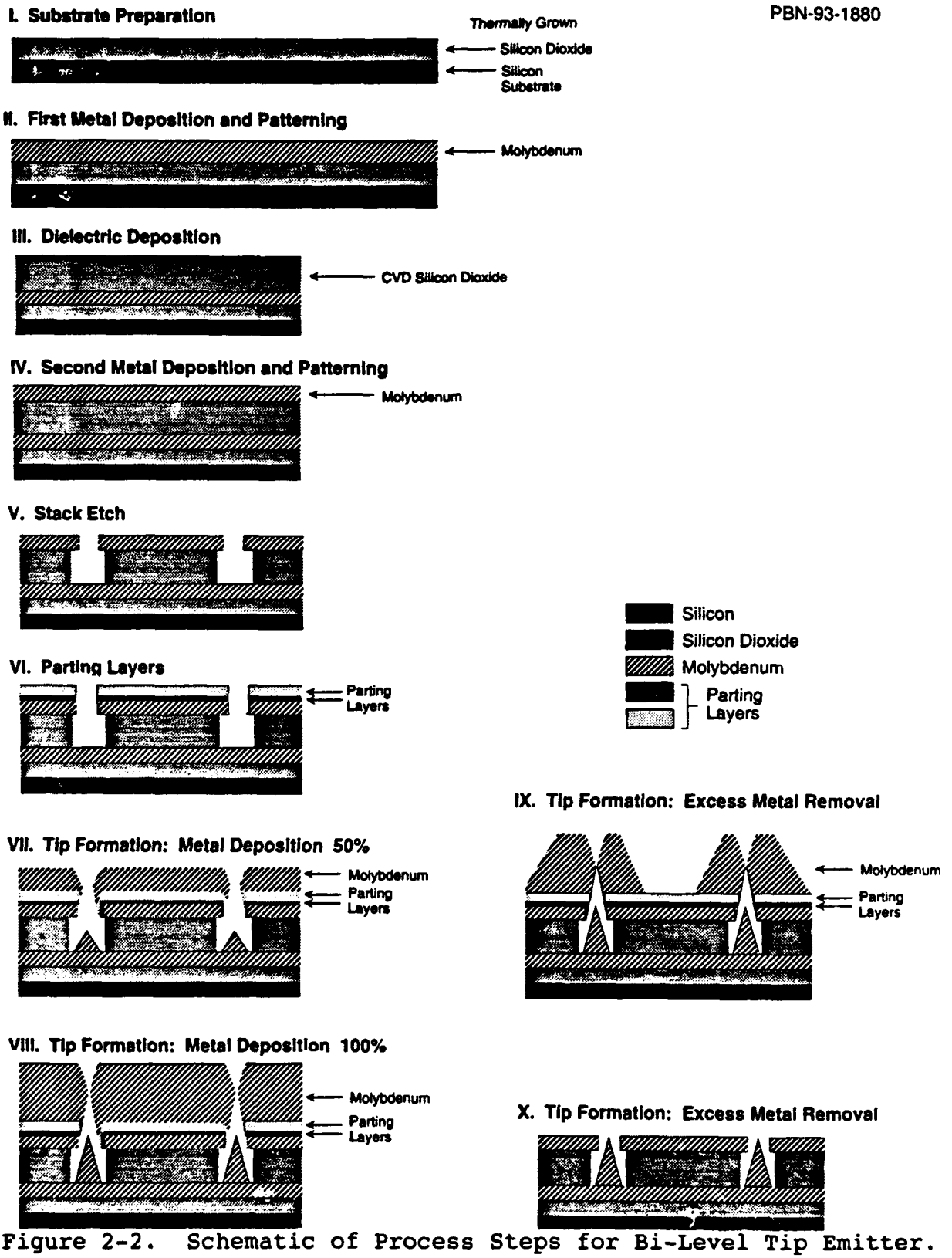


Figure 2-2. Schematic of Process Steps for Bi-Level Tip Emitter.

For a silicon substrate a blanket SiO_2 layer is grown for insulation (Figure 2-2, Step I). For a sapphire substrate, this step is not required. Next, a molybdenum layer (M1) is deposited by sputtering and then patterned (Step II). A blanket SiO_2 dielectric layer (D1) is then deposited by Chemical Vapor Deposition (CVD) (Step III). The top moly layer (M2) is then deposited and patterned to form the gate electrode (Step IV). The top metal is then masked to define the cavities and then the stack is then is vertically etched by a reactive ion etch (Step V) to form cavities about 1 μm in diameter. Next, the surface is coated and the upper sidewall (not the lower sidewall of the cavities) by a low angle evaporation with a set of stress relief and release layers (Step VI). To form the tips, approximately 1.5 μm of molybdenum is evaporated onto the substrate. The molybdenum forms a cone in the cavity due to a gradual closure of the cavity opening (Steps VII and VIII). As the tip material is evaporated, it coats the top of the release material and the sides of the metal aperture defining the cavities at the emitter sites. Since the aperture sidewalls are continually coated as the tips are formed, the opening at the top of the cavity becomes gradually smaller resulting in the conical shape of the tip. After tip formation, the excess molybdenum is selectively removed by dissolving the release layer (Steps IX and X). More details of some of steps are discussed below.

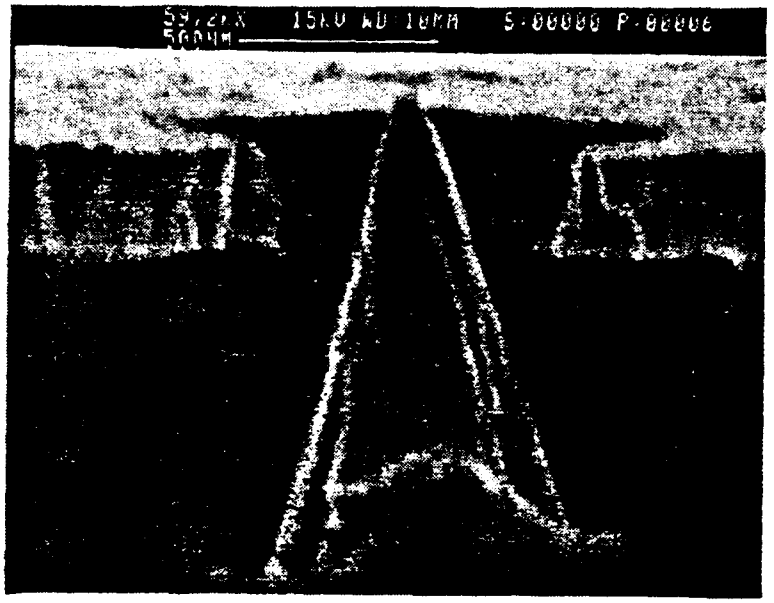
The M1 and M2 metalizations are patterned for interconnect. At crossovers, there is a step. It was found that the M2 layer was cracking at this edge. The D1 depositions step was modified to solve this problem. First 1,000 angstroms of LTO (low temperature oxide) is deposited. This is followed by 8,000 angstroms of phosphorous oxide doped LTO. The dielectric is then re-flowed to smooth out the steps. This is followed by a final 1,000 angstroms of LTO. The addition of these process steps eliminated the crossover cracking problem.

Reactive ion etching is required to etch the cavity in Step V. For the standard tip emitter, two layers must be etched; they are one 3,000 angstroms layer of molybdenum and one 8,000 to 10,000 angstroms silicon oxide layer. A multistep etch, based on alternate chlorine and fluorine chemistries for molybdenum and silicon oxide etching, was devised. There are no constraints placed on the molybdenum-to-oxide etch rate ratio since there is no strict requirement that the molybdenum etch stop on oxide. However, the oxide etch requires good selectivity to molybdenum so that the bottom layer of molybdenum is not etched into after the last oxide layer is etched away and that the top moly layer is not etched after the photoresist has been eroded away.

The height of the tip made in Steps VII and VIII is determined by the diameter of the hole. If the hole is too small, the tip will be below the gate and if the hole is too large, the tip will be above the gate. The lithography of the hole diameter is controlled to within plus/minus 0.1 micron. Even if the hole diameter is controlled, variations in the dielectric thickness will effect the placement of the tip relative to the gate. Figure 2-3 shows these two cases.

Due to the thick layer of molybdenum necessary for the tip formation (Steps VII and VIII), peeling and cracking due to the induced stress was found in M2 after the excess molybdenum was removed. This problem was resolved by modifying the release layer to include an additional layer that stopped the stresses from propagating down to the M2 layer.

Initially, there were many shorts between the two metalizations on the first wafer lots. It was found that the shorts were there even if the tips were not deposited. The culprit was the residues left from the RIE of the holes (Step V). An improved hot solvent clean solved the problem.



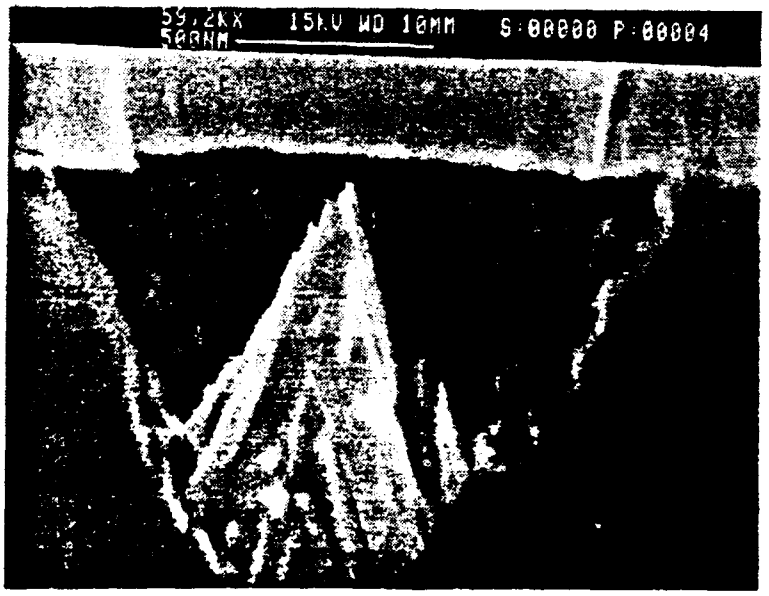


Figure 2-3. (Top) Tip Above Gate and (Bottom) Tip Below Gate.

2.3 Circular Edge Emitter

There was a second process development effort to fabricate fine circular edge emitters. First, using an oxidized silicon or sapphire wafer the same metal-oxide-metal layers used in the tip process are made. The appropriate gate and emitter electrodes are patterned in this step. Then a 5,000 angstroms oxide inverted mandrel layer is deposited and a 2,000 angstroms titanium layer is deposited. Next, micron-sized holes are patterned where the emitters are desired. The titanium and oxide layers are reactive ion etched and the resist stripped. The titanium is now the mask for further etching and the cylindrical opening is the inverted mandrel for the circular edge. Half of the top moly layer is back-sputtered onto the oxide mandrel and the remainder is etched by RIE. Finally, the oxide mandrel is etched away. Figure 2-4 is a SEM of one of these structures from an oblique angle and Figure 2-5 shows an array on six micron centers. Figure 2-6 shows a structure in cross section. The fine edge is on the order of 100 angstroms wide and quite uniform.

In reverse to that of the tip field emitters, the gate is the bottom electrode and the emitter is the top. Gate voltage will generate an electric field that will spread through the central hole and in theory create field emission from the edge. In practice, no emission currents were found. This work was then discontinued and all our process development efforts were on the tip type of emitters.

2.4 Specialized Process Equipment

A major capital investment was made in a custom evaporator for this program. The unit features two 30 cc four-pocket electron beam hearths for individual or co-evaporation; six head quartz crystal and electron impact spectroscopy disposition monitoring; three-inch MBE manipulator with programmable substrate rotation and azimuthal control; gridless low energy ion source for

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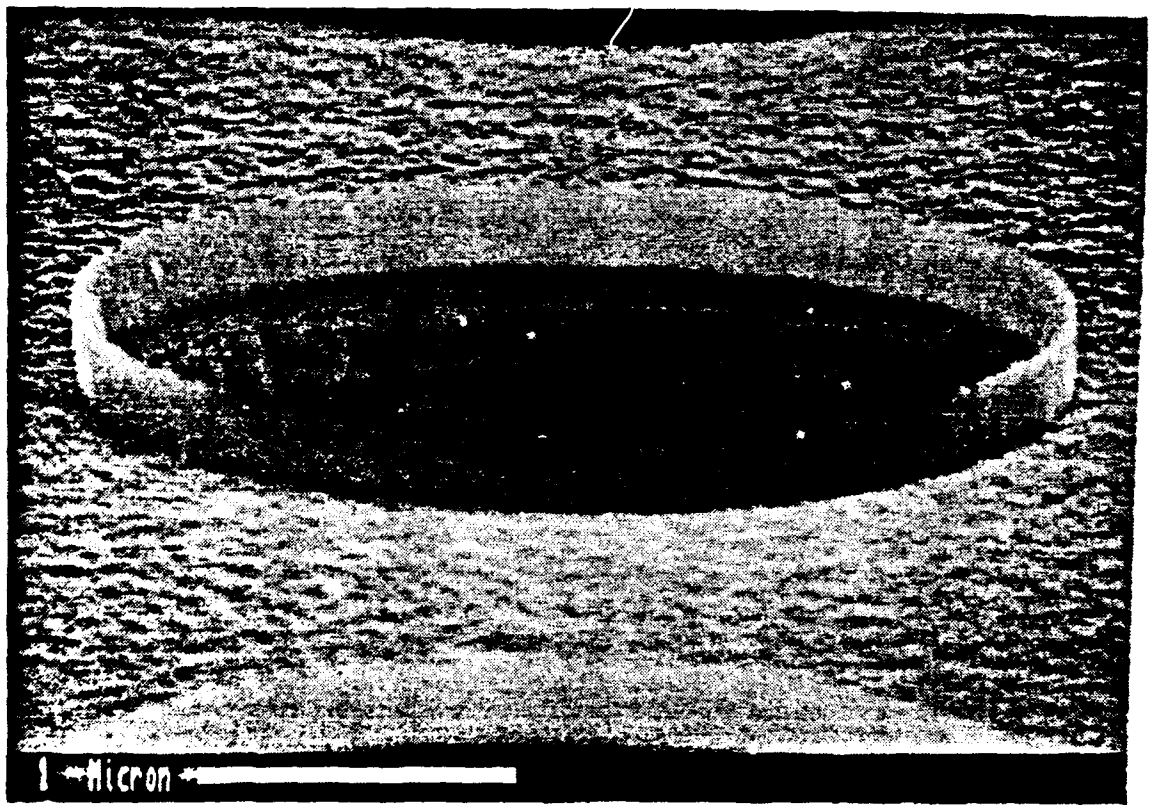

Figure 2-4. Single Circular Edge Emitter.

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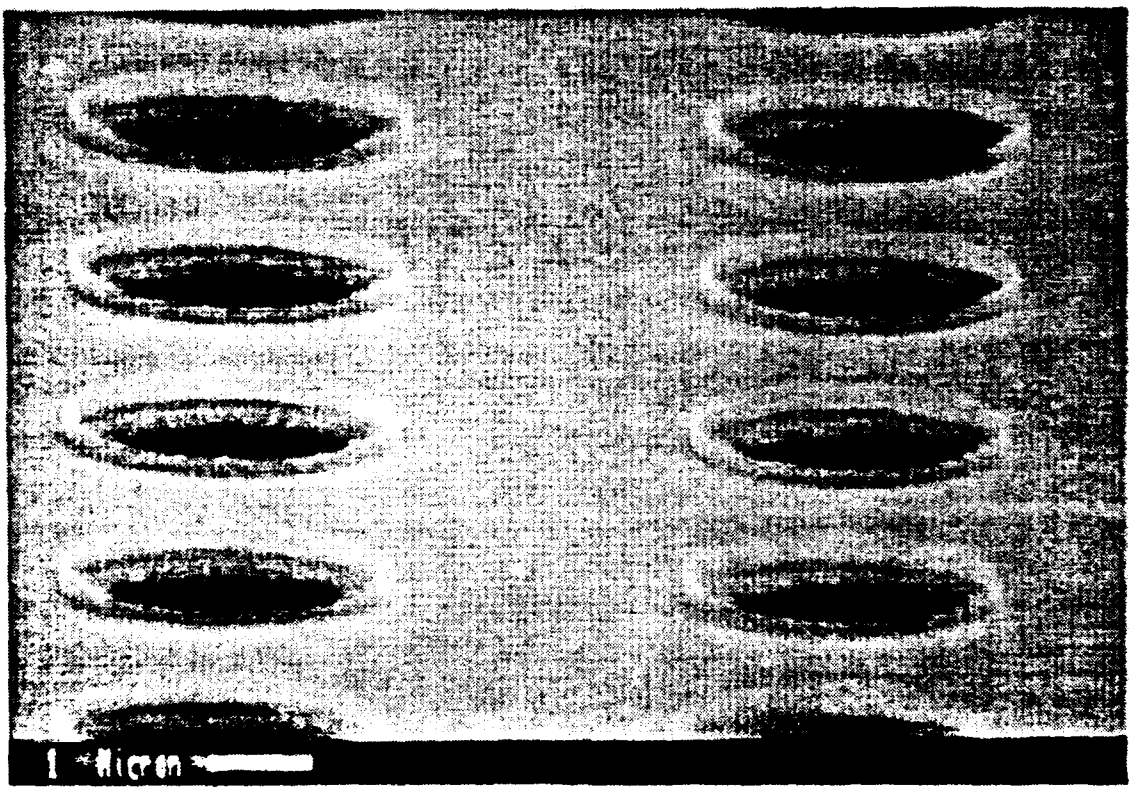

Figure 2-5. Array of Circular Edge Emitters.

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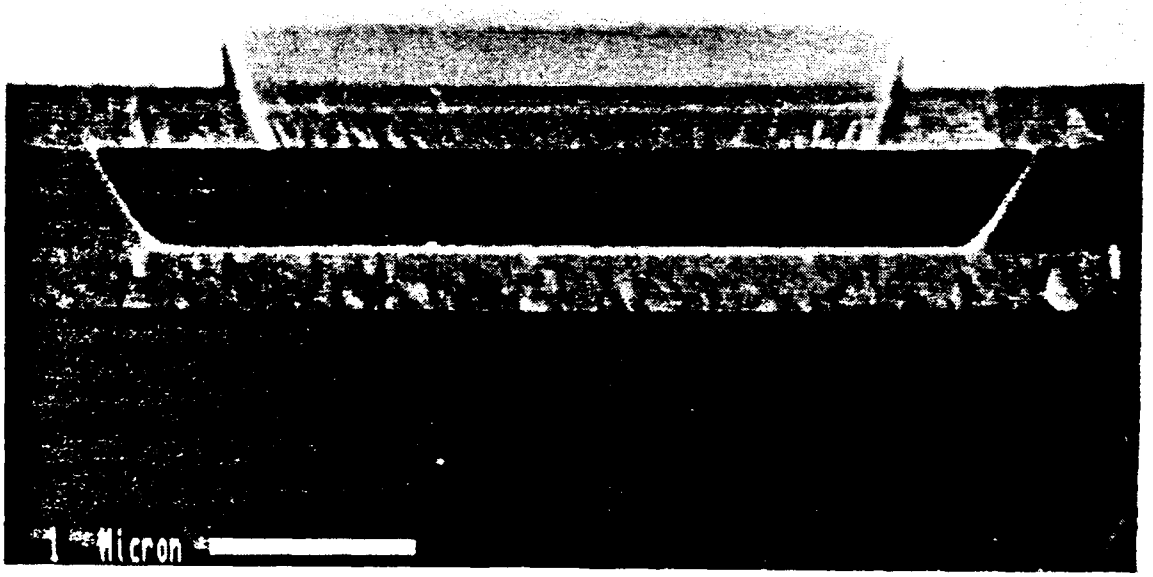

Figure 2-6. Circular Edge Emitter in Cross Section.

substrate pre-clean or reactive co-deposition; RF sputter source; load lock and prep chamber with substrate bakeout up to 450°C; and a 36-inch throw. The unit is fully operational and is used for all the evaporation steps in FEA cathode fabrication. The unit is shown in Figure 2-7.

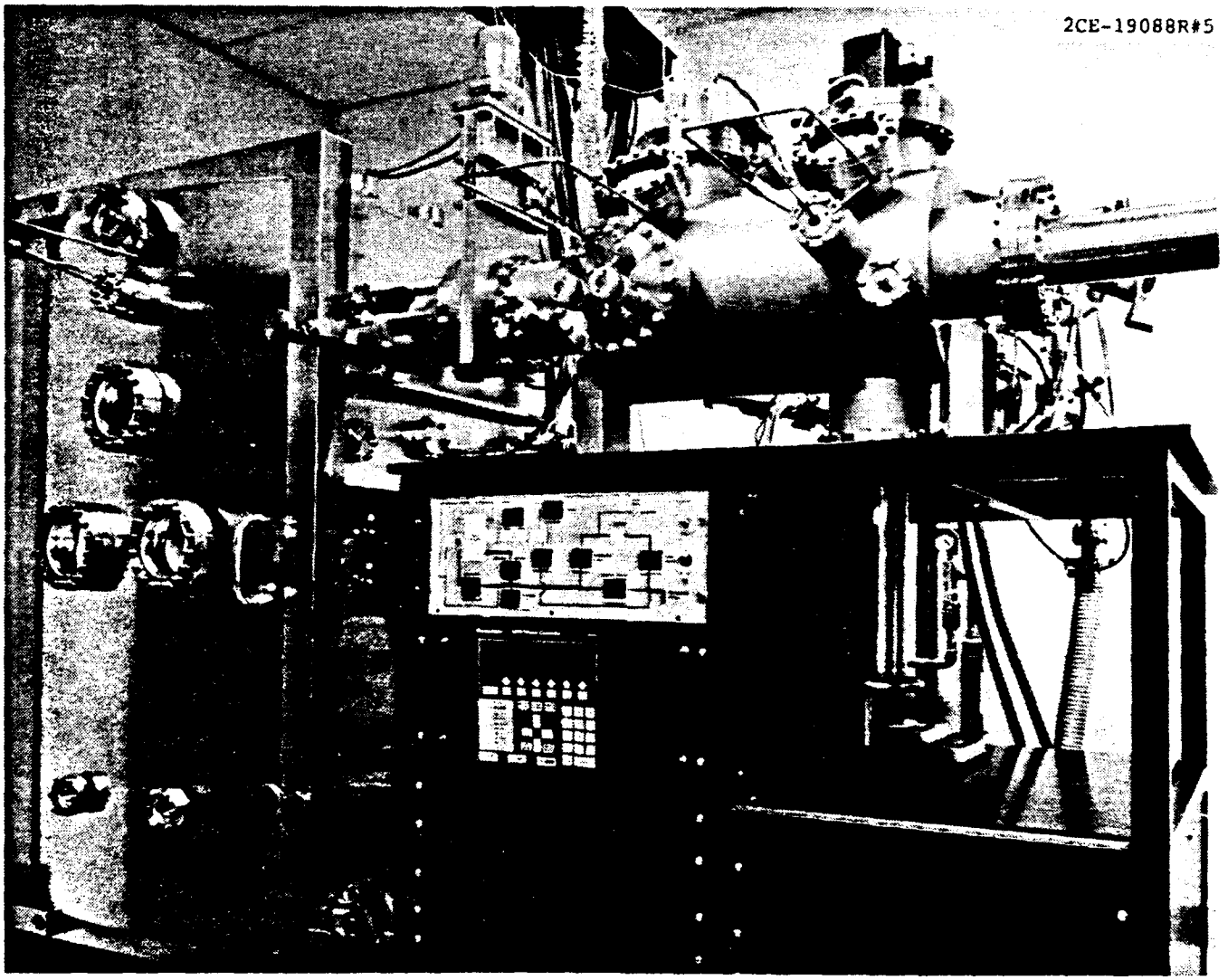

Figure 2-7. Custom Evaporator with Load Lock and Prep Chamber.

3.0 TEST TRIODES

3.1 Overview

The electron emission from field emission cathodes is modeled with the Fowler-Nordheim Equation given below.

$$I = aV^2 \exp(-b/V) \text{ (amps)}$$

where

$$a = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B\ (1.44 \times 10^{-7})}{\phi^{1/2}}\right]$$

$$b = 0.95B\phi^{3/2}/\beta$$

$A = 1.54 \times 10^{-6}$

α = emitting area

$B = 6.87 \times 10^{-7}$

β = field enhancement factor at surface

ϕ = surface work function

By taking the derivative with respect to V, g_m may be obtained

$$g_m = \frac{\partial I}{\partial V} = \frac{I}{V}\left[2 + \frac{b}{V}\right] \quad \text{(Siemens)}$$

The two parameters **a** and **b** fully specify the functional form. The term **a** scales as field enhancement due to curvature and the closeness of the gate electrode. This term is on the order of 1.5 x 10^{-6} amps/volts^2 per tip and needs to increase for improved performance. The term **b** scales, as the surface work function, is on the order of 1000 volts and should decrease for improved performance. The conventional way to plot data is I versus 1000/V. Fowler Nordheim I/V performance will appear as a straight line with this scale for the typical field emission parameters encountered in this study. Also on this type of plot, the farther the curve is to

the right (larger 1000/V, decrease in **b** term) and the more vertical (increased I for a given V, increase in **a** term), the better the device.

As opposed to solid state devices, the "processing" of FEAs is not complete after the chip comes of the fabrication line. After the wafers are diced into chips, they are H_2 (atmospheric pressure) fired at 400 degrees centigrade for 20 minutes. The chips are kept in a dry N_2 atmosphere whenever possible. The bonding and final assembly are done in air. The initial turn-on is not instantaneous. The voltage is gradually increased over at least 24 hours before getting full current. This turn on may be though of as a continuation and the final step of the "processing".

Two test vehicle approaches were used to evaluate high frequency FEA performance. The first approach is a planar cathode in a test chamber. The second is a cylindrical micro-triode tube.

3.2 Planar Triode (MMIC) Approach

3.2.1 Test Stand and Chip Layout

To test these arrays electrically, it is necessary to bake and test them in ultra-high vacuum. A test station for this purpose has been fabricated under company funds. The device under test is bonded to a ceramic circuit board, which contains metal leads which are wire-bonded to the FEA and, through a vacuum feedthrough, connect to electrical power supplies and RF measuring equipment. The vacuum system is bakable to 450°C. We also are able to test more than one chip at a time. The test stand is shown in Figure 3-1.

The pumping system consists of a sorption pump, followed by a turbo pump and then a vac-ion pump. There is no mechanical oil fore-pump in the system. The system is capable of vacuum on the 10^{-10} Torr. There is a residual gas analyzer and a microscope for

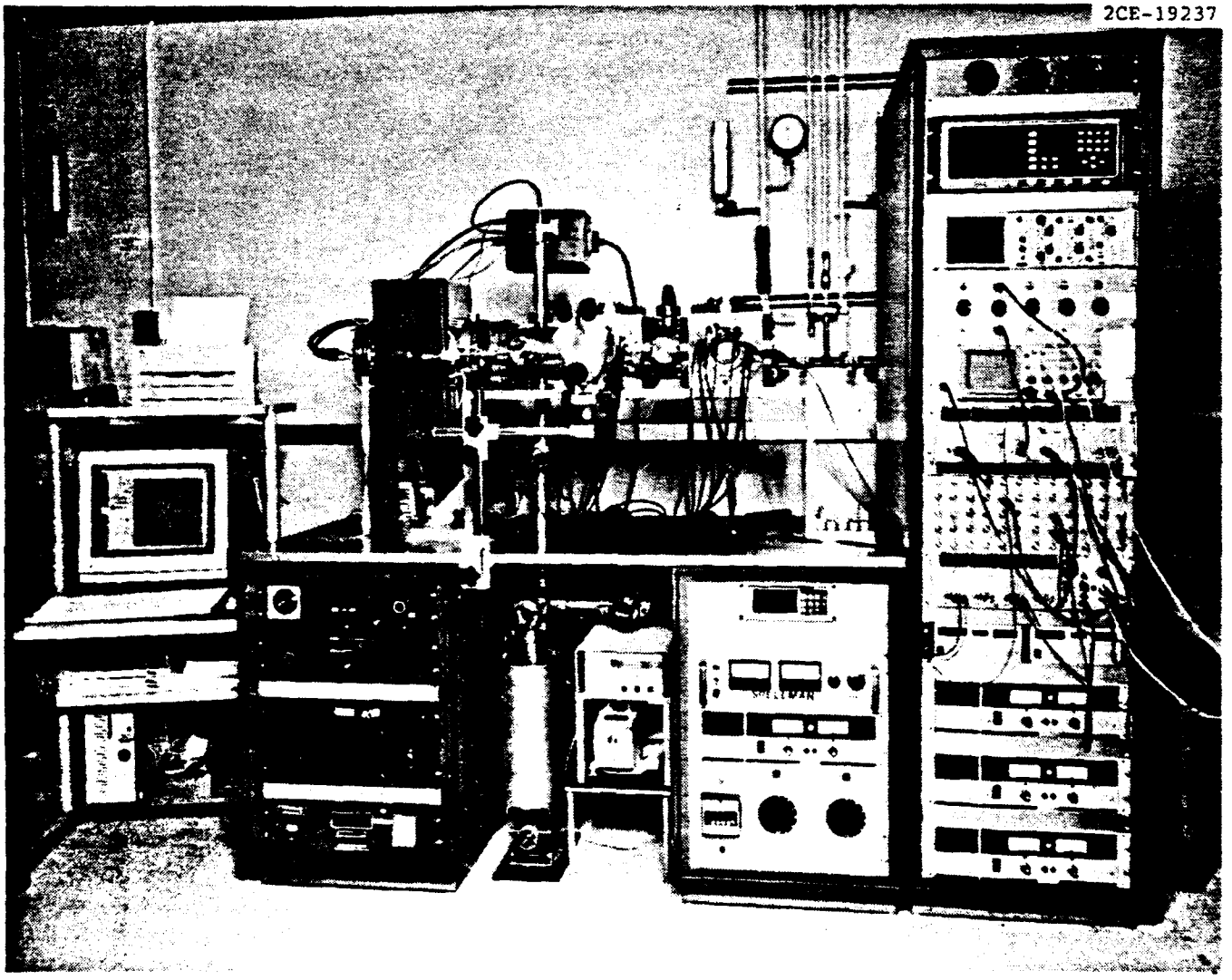

Figure 3-1. Custom UHV Compatible FEA Test Stand.

direct viewing through a window. The power supplies allow operation up to 10 KV although most tests were performed under 2 KV. There is also a moderate voltage (250 volts) gate pulser that allows for low duty operation. Most of the equipment is able to be controlled by a computer. The bakeout sequence, the initial device turn on, and the measurement of I/V characteristics are under program control. Figure 3-2 shows a typical bakeout run. The layout of the first iteration planar chip is shown in Figure 3-3.

The chip size is 3 mm square. It has seven bondable devices plus an additional five RF probeable structures. The top device is a two-port structure to allow for "tuning". The balance of the devices are one port. The bonding pads along the sides are in a ground-signal-ground configuration with a shared ground. They are gold plated to allow for bonding to the alumina. The pitch of these pads is 300 microns. Closer into the devices are RF pads on a 100 micron pitch. The dc/low frequency alumina is shown in Figure 3-4.

The alumina is 2.5-inches square. The planar triode chips fit into the lower (larger) depression. This allows the wire bonding to be flush and eliminates the high voltage at the chip edge. The alumina is mounted on a test flange that itself mounts on the test chamber. Wires are bolted to the alumina and then lead to the vacuum feed-thru's on the flange. A heater is placed on the backside of the alumina. The anodes were made from a variety of materials including stainless, copper, and molybdenum. The fired moly anodes appeared to give the results. For the high current tests, we were worried that the anode might be the limiting element for proper operation; therefore, high current tests were performed at low duty cycle. The cathode anode spacing was typically 1 to five mm. For all the tests of the planar triode, the device was configured in a common emitter configuration with the emitter grounded, the anode at a positive high voltage and the gate driven positive to turn the device on.

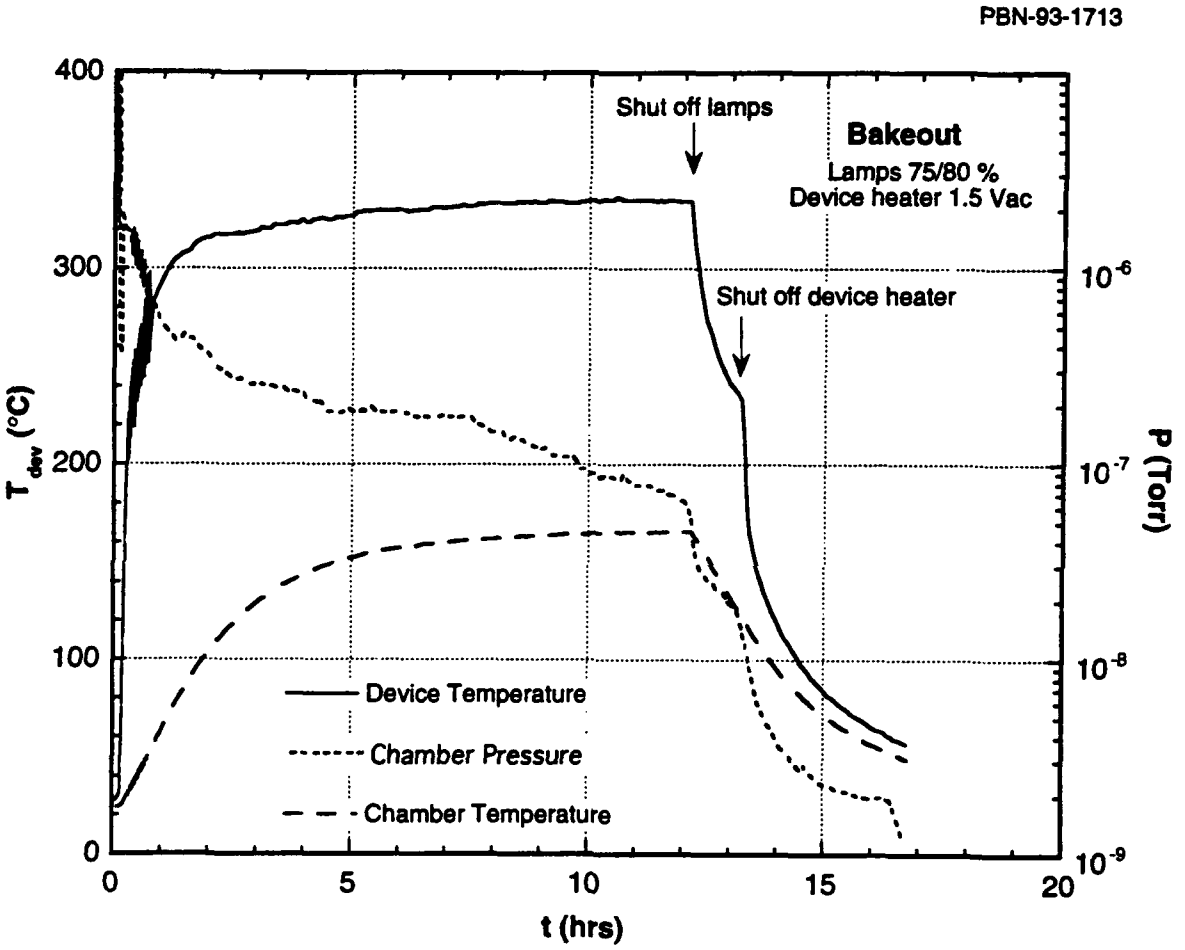

Figure 3-2. Computer Controlled Bakeout of Test Chamber.

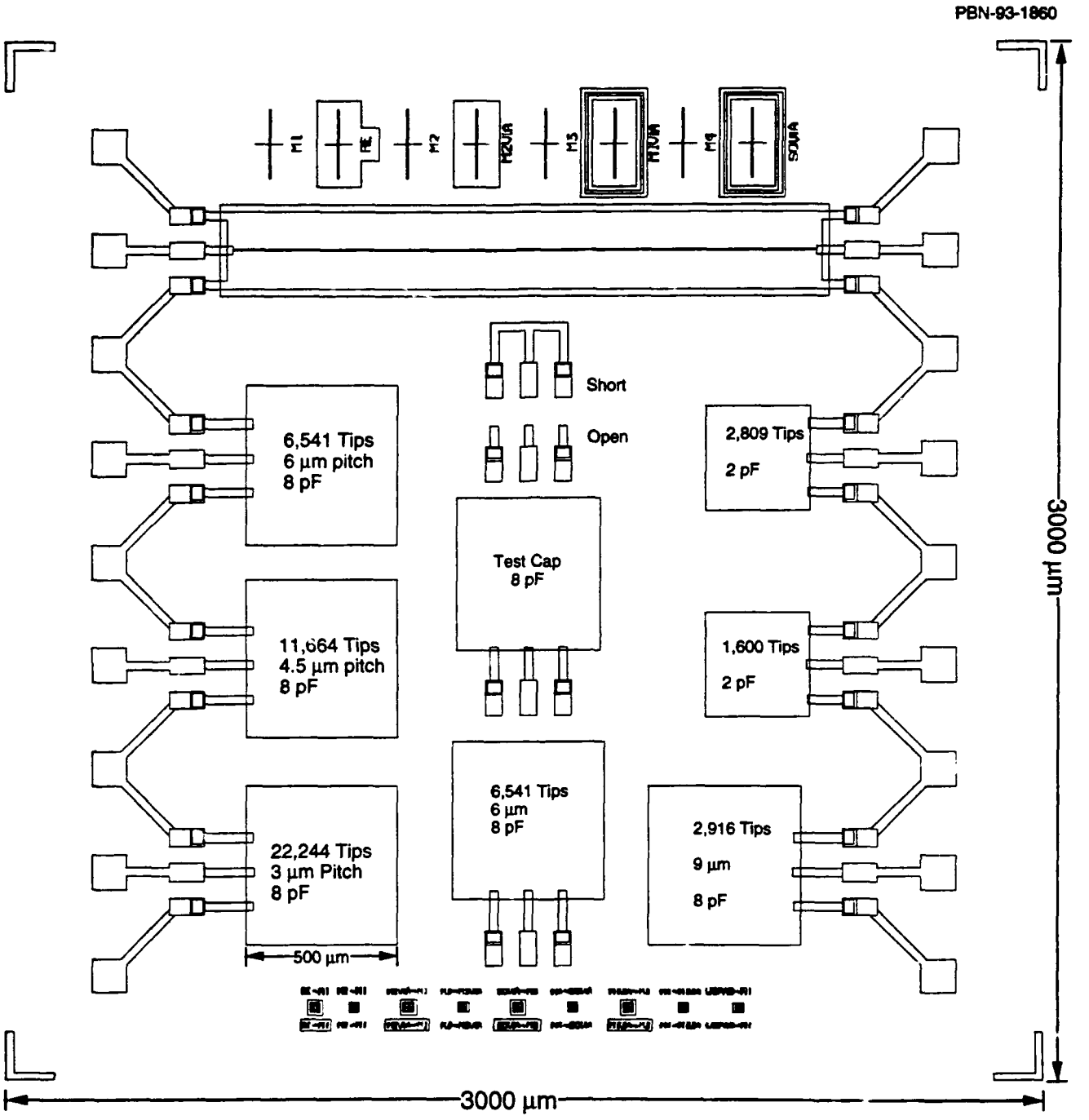

Figure 3-3. Layout of First Iteration of Planar Triode Cathode Chip.

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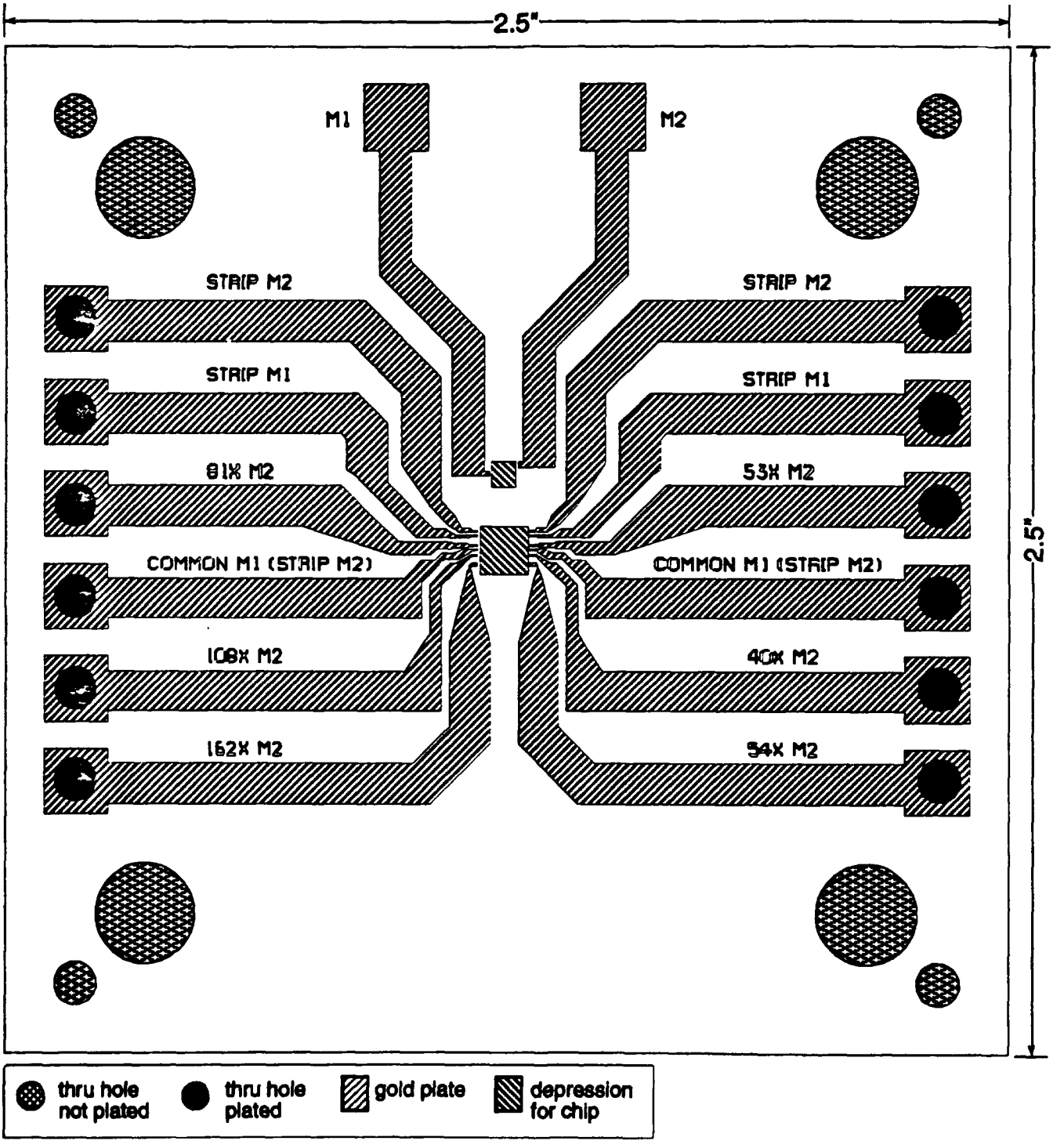

Figure 3-4. DC Test Alumina for Cylindrical and Planar Triode Cathodes.

3.2.2 DC Results

A composite Fowler-Nordheim plot of typical performance data is shown in Figure 3-5.

The ⊞ and o data are from chips that used mask developed under company IR&D funds. As can be seen by a variety of the curves, the total current goal of 5 milliamps at a gate voltage less than 250 volts was met. The emitting area for the ⊞ and o data (from the contract mask) is 0.05 cm squared. The total current required to meet the current density goal of 5 amps/cm^2 is 12.5 ma. Both these curves exceed that value. The data is also presented normalized to the number of tips in Figure 3-6.

The best performance obtained was 14 micro-amps per tip. From the spread in the data and from other single tip measurements, the current is not equally spread out over the tips. Because of the exponential form of the emission and the lack of any current limiting resistors (ballast), we suspect that only a percentage of the tips are carrying the current. Therefore, the actual peak tip current load could be much higher.

The dc g_m normalized per tip data is shown in Figure 3-7.

The 2 micro-Siemens per tip value is close to what is required to meet the F_t goal of 1 GHz. The goal was not met.

The best current performance seen in the planar configuration is shown in Figure 3-8.

This was a 5000 tips array that gave 14 micro-amp per tip and 0.8 micro-siemens per tip. This device was operated at 2% duty and was on a sapphire substrate.

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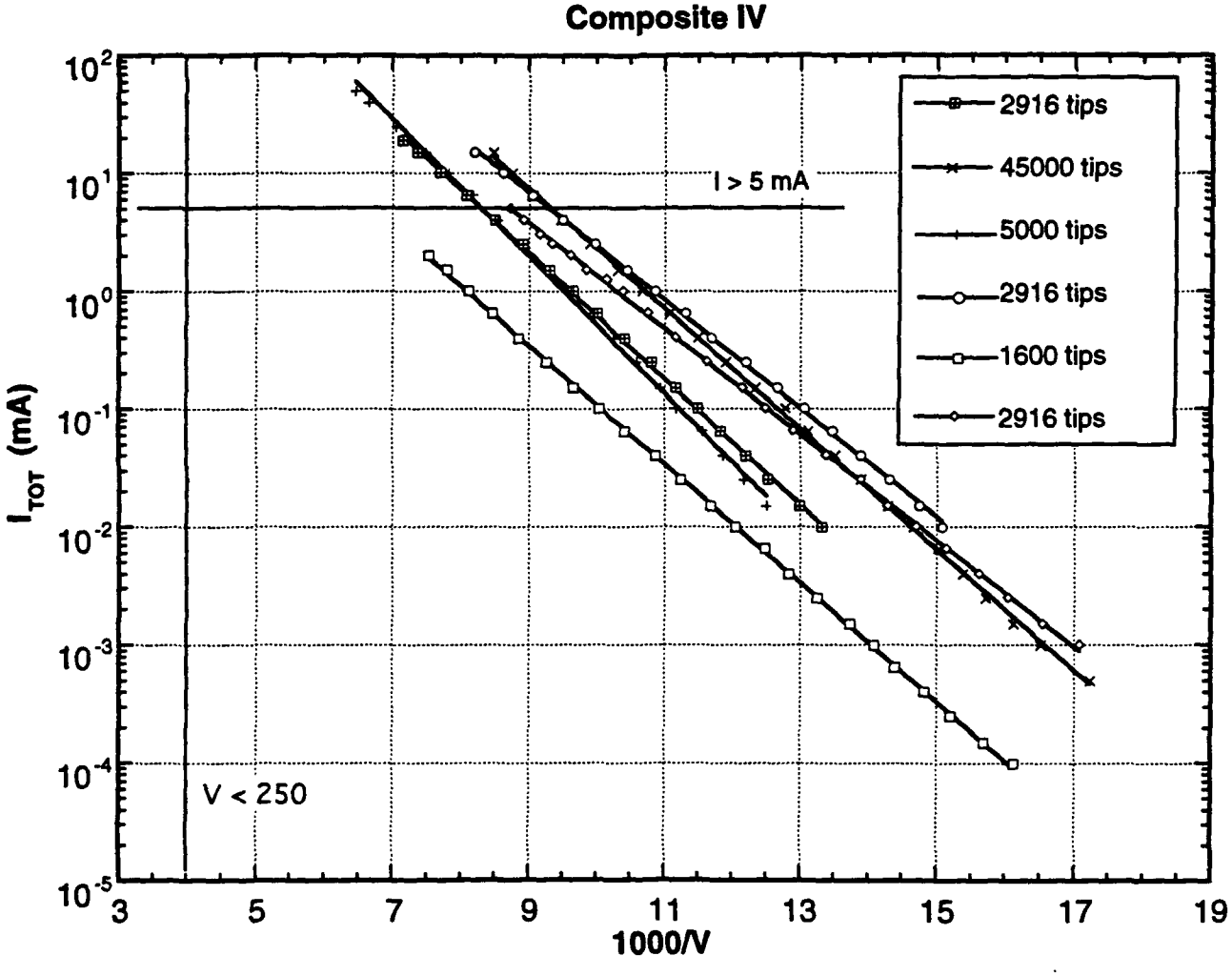

Figure 3-5. Composite Fowler-Nordheim Plot of Typical Data - Total Current.

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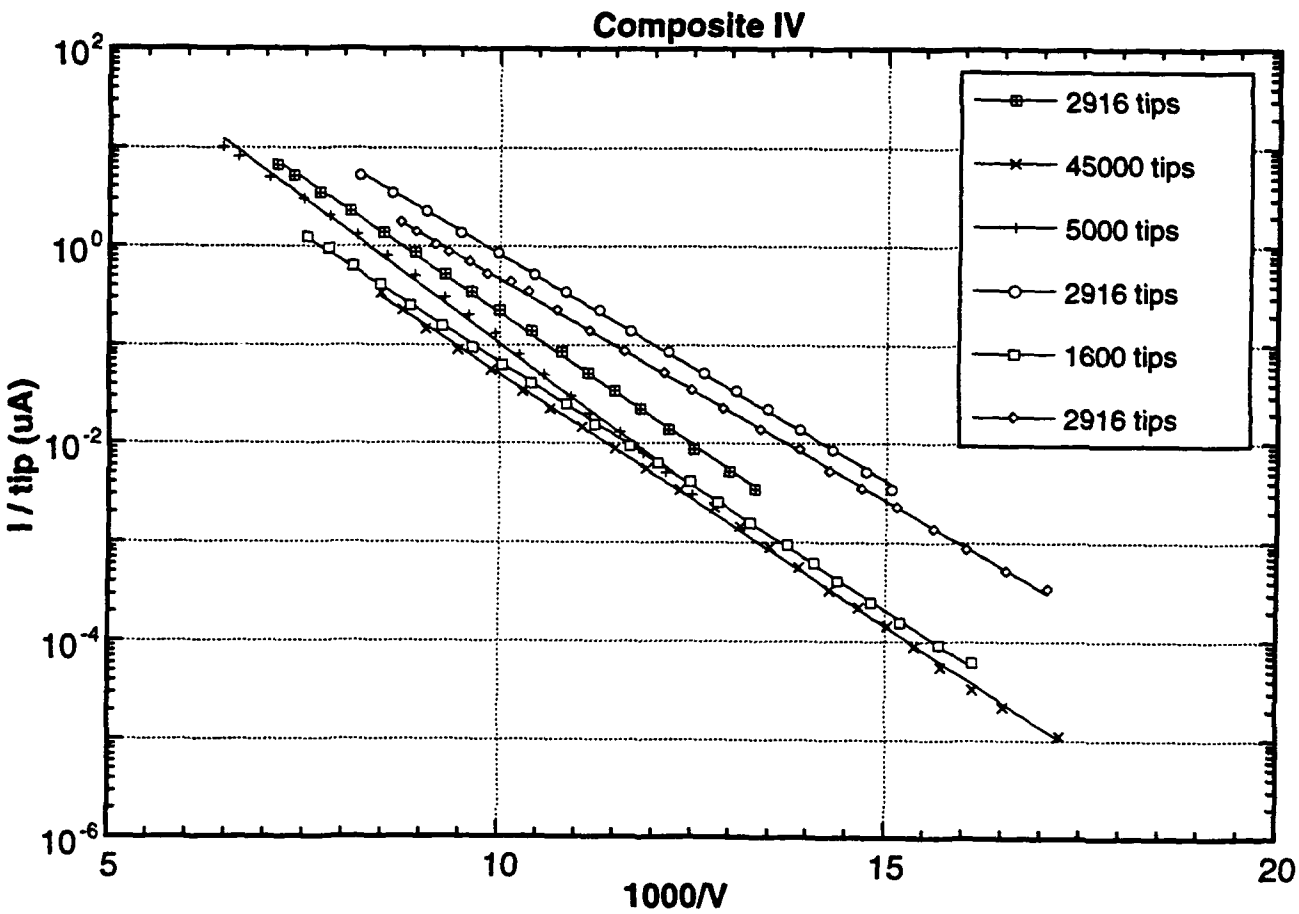

Figure 3-6. Composite Plot - Current per Tip.

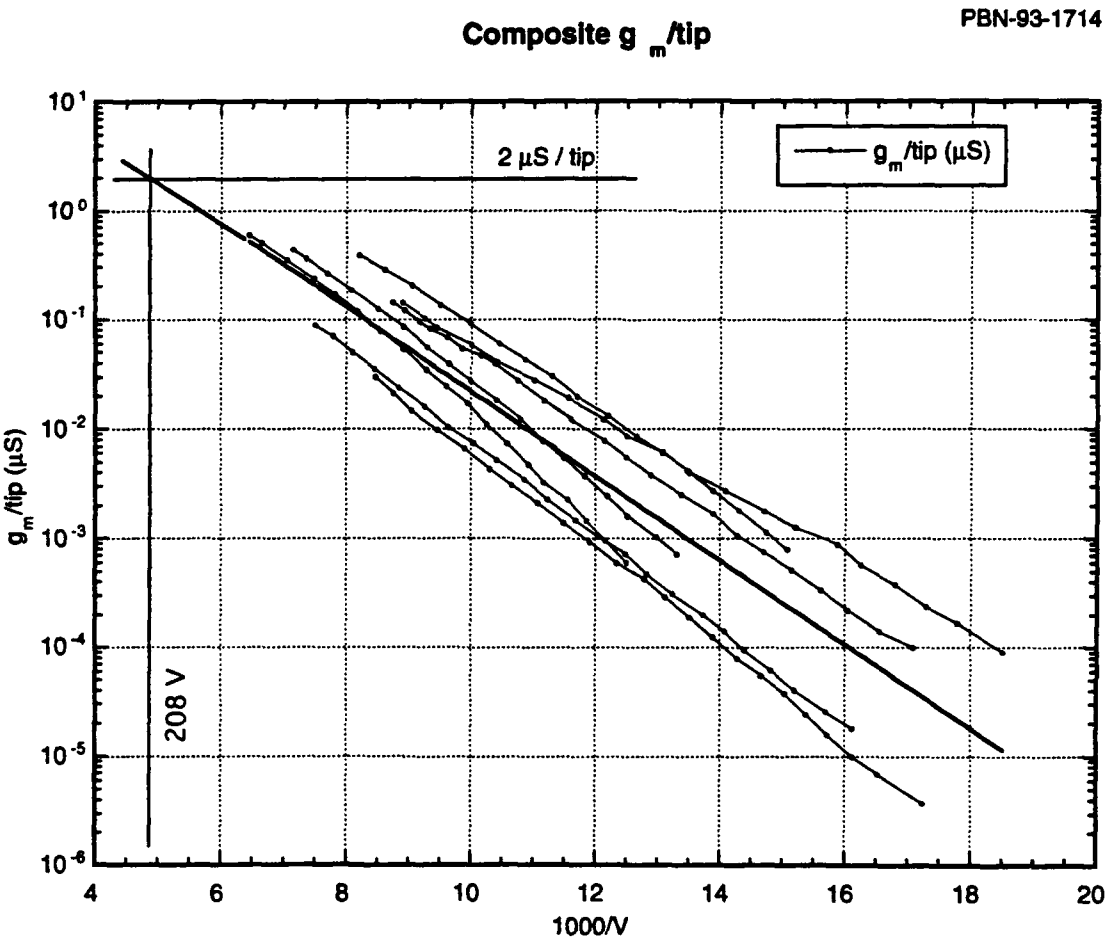

Figure 3-7. Composite Plot - Transconductance per Tip.

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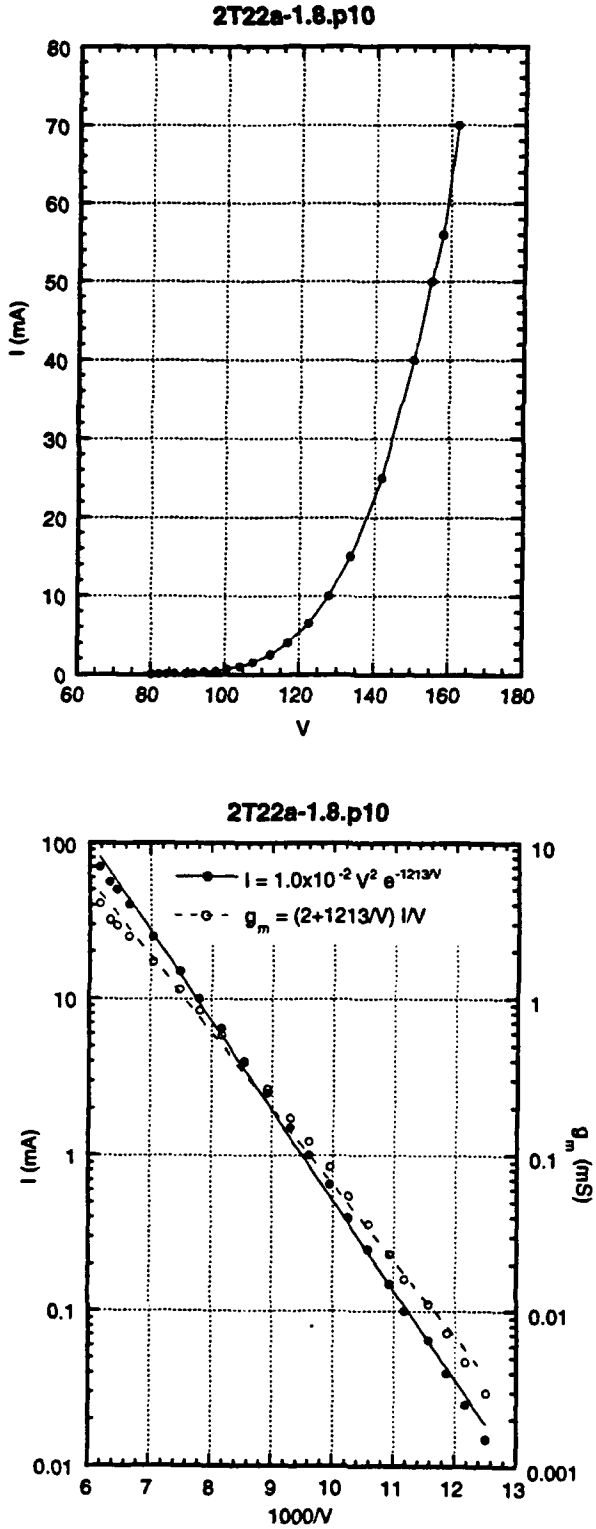

Figure 3-8. IV Plot of Highest Current Device.

The data presented above was all at anode voltages between 500 and 1000 volts. The transfer characteristics of a typical device is shown in Figure 3-9.

This data looks more like conventional tube pentode data as opposed to triode data. This can be explained by the fact that the gate to emitter spacing is much smaller than the gate to anode spacing. Therefore, the anode voltage does not effect the anode current except when it is near or less than the gate voltage. At these low currents, there are no space charge effect. At the current levels anticipated to meet the F_t requirements, space charge will be a consideration.

3.2.3 RF Results

The test flange and alumina used for the dc/low frequency testing does not work above frequencies of 10 MHz. A high frequency flange and alumina were fabricated that work up to 10 GHz. The high frequency flange is both bakable to 450°C and UHV compatible. It features four RF leads for the cathode, one anode lead, and a variety of dc leads for bias, heaters, etc. The unit without the alumina in place is shown in Figure 3-10. The high frequency alumina layout is shown in Figure 3-11.

The four coaxial cathode leads are clamped to the co-planar lines that are tapered down to the chip maintaining a constant 50 ohm impedance. The anode cantilevers over the cathode from the bottom. The additional ground beneath the anode was added for improved RF match. The chip has four leads per side while the alumina has only two. This is because of space limitations. Therefore, the chip may be slid up or down in the depression to choose the first and third or second and fourth row.

Modulations of a simple triode at low level have been observed with our first iteration of planar triode chips. A square area of 0.5 mm square with 26,244 tips was run at 150 micro-amps at 72.3 gate voltage and 500 volts on the anode. This was performed CW so

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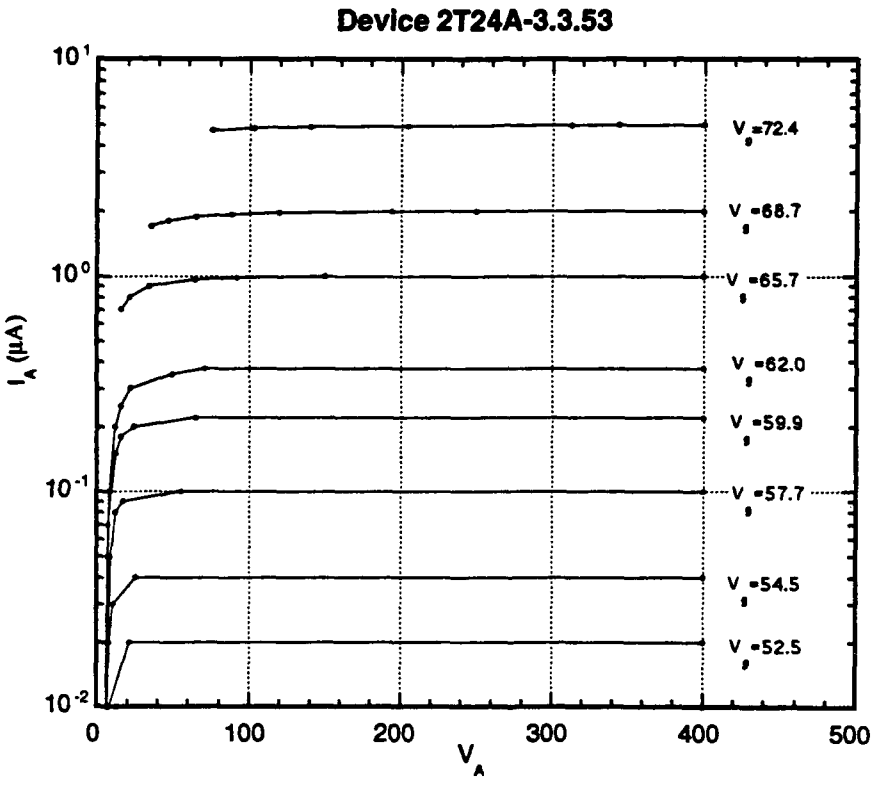

Figure 3-9. Low Current Transfer Characteristics.

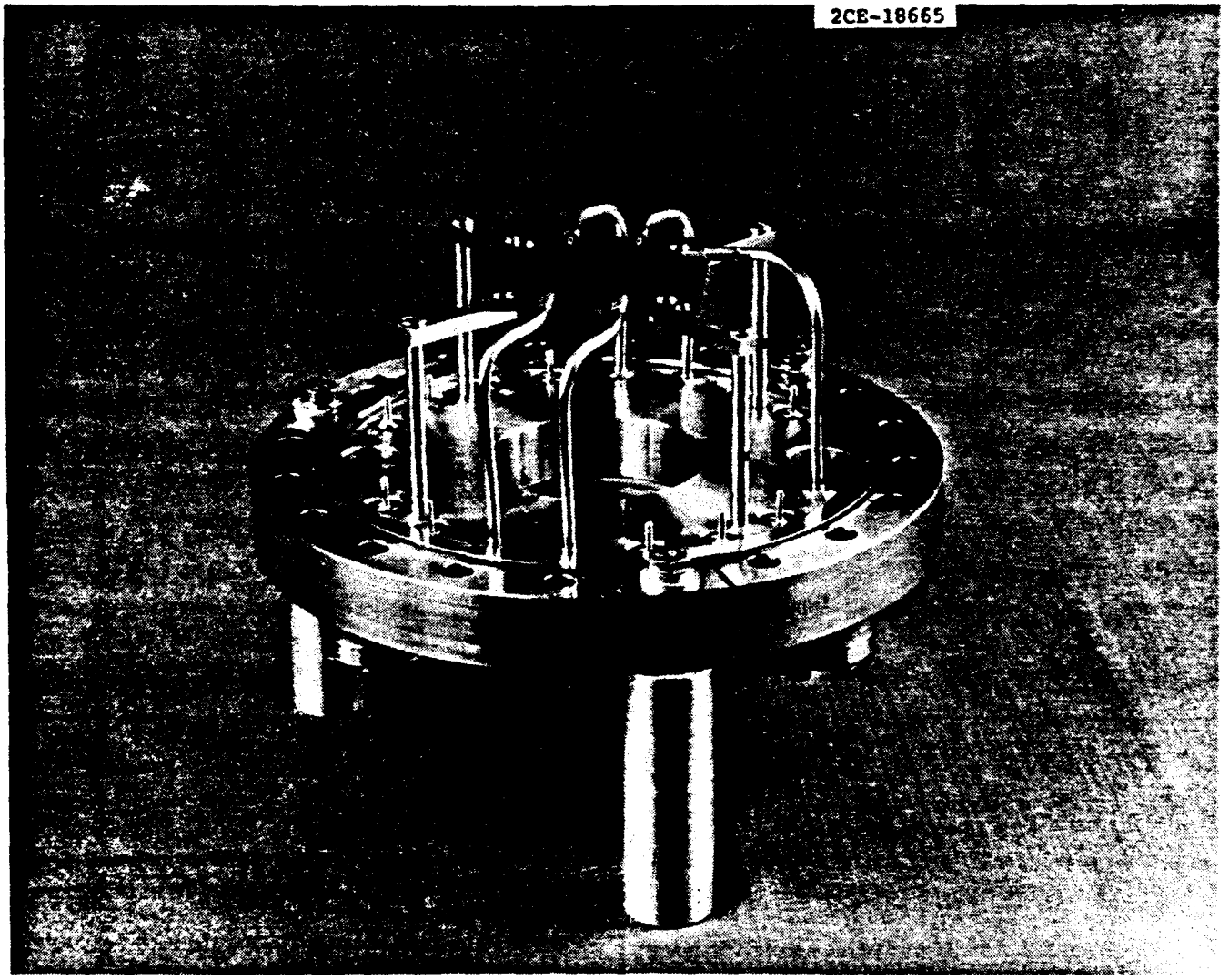

Figure 3-10. High Frequency, Bakeable, UHV Flange.

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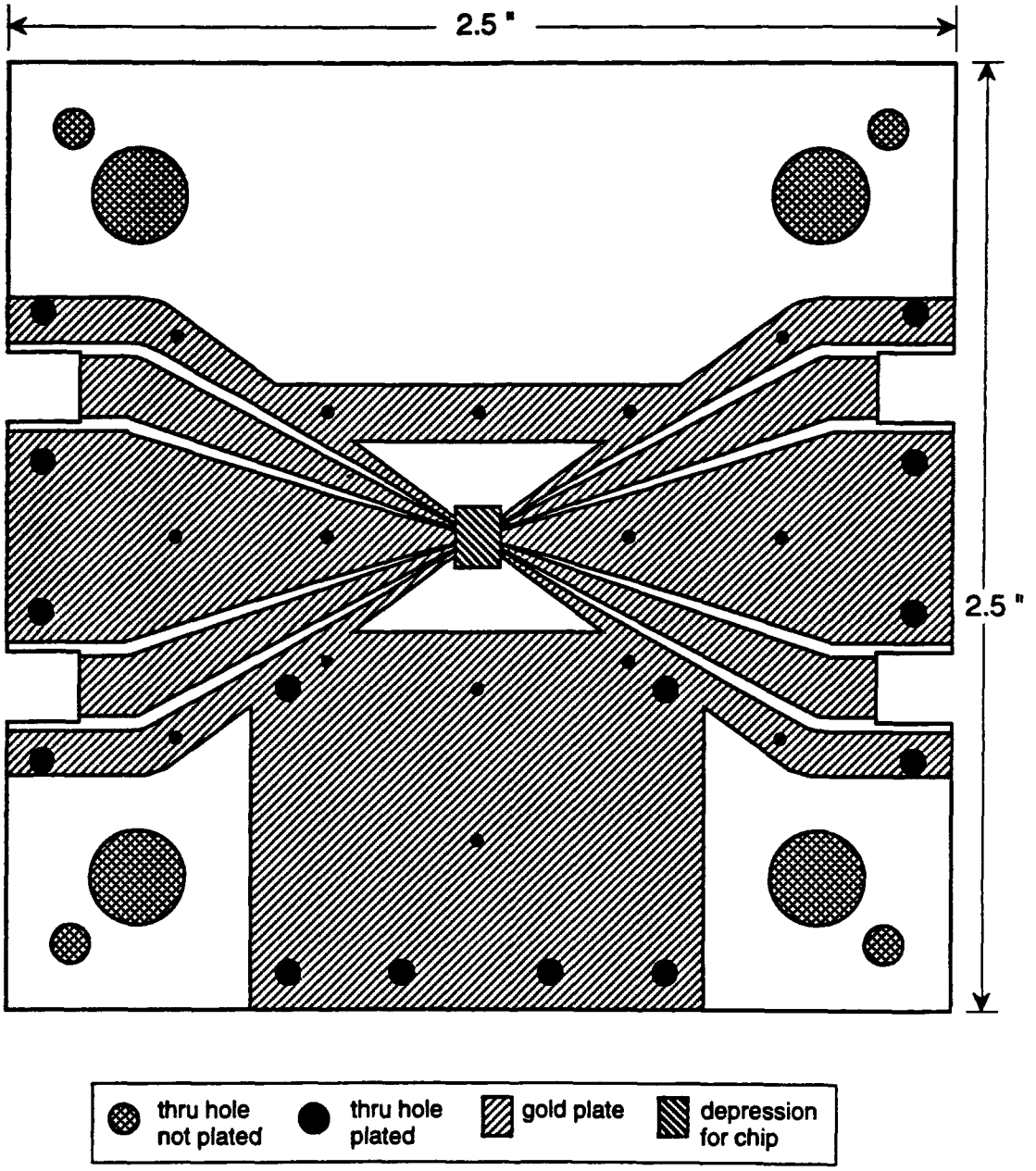


Figure 3-11. Layout of High Frequency Alumina.

the Vector Network Analyzer (VNA) could measure the S-parameters (a pulsed VNA is not available in our lab). The equivalent circuit for the tests are shown in Figure 3-12.

The source and load are in the VNA. The bias-T circuits combine the RF signal with the dc bias voltage while isolating the source and load form the high voltages. The operating bandwidth of the bias-T is 30 MHz to 3 GHz. The results were not de-embedded to the device plane and therefore include the parasitics of the alumina and the flange. The gate capacitance includes 8 pF from the chip and 2 pF from the alumina. The anode and isolation capacitance is due to the parasitics of the unshielded anode geometry. There is also an input resonance due to the cavity of the chamber that is not included in this equivalent circuit.

The four S-parameters of the device are shown in the off and on state in Figures 3-13 to 3-16.

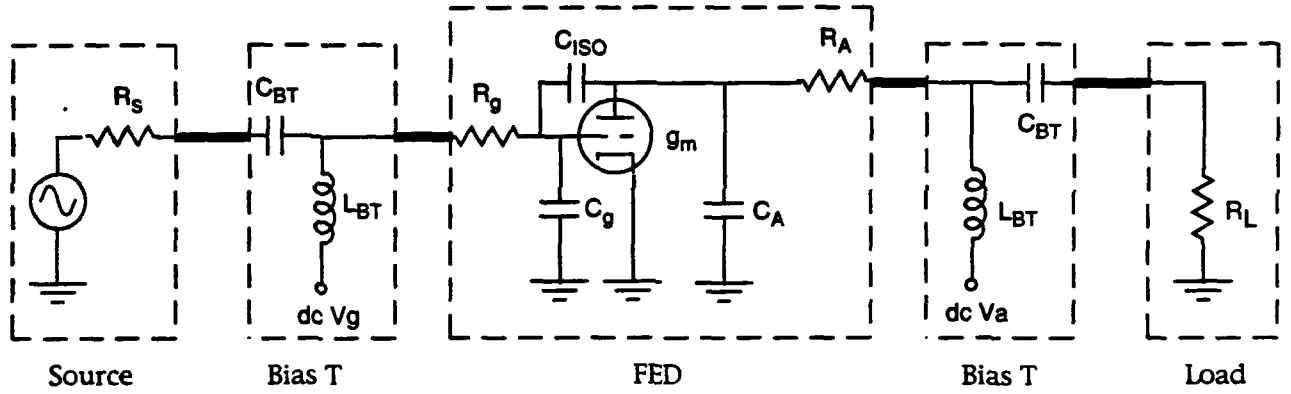
Since the device is highly mismatched on the input and output in a 50 ohm system and is relatively low gain, only a differential change in insertion loss is seen on the S_{21} curve (Figure 3-14). The fact that S_{21} shows a change while S_{12} does not change when the device is turned on indicates a true gain mechanism and not just a variable attenuator. Because of the resonance, feedthrough due to the isolation capacitance is not seen clearly above 0.30 GHz. Since on the S_{21} data, the hot curve is above the cold curve up to 1 GHz indicates that modulation is occurring (albeit weakly) up to that frequency.

3.3 Cylindrical Triode (Tube) Approach

The cathode for the micro-triode is a 700 micron annulus with seven concentric circles of 714 tips per circle for a total of 4,998 tips and a calculated parallel plate capacitance of 1.55 pf. The layout of the cathode is shown in Figure 3-17.

PBN-93-1711

Equivalent Circuit For Planar Triode Tests



$R_S = R_L = 50\ \Omega$
$C_{BT} = 1000$ pF
$L_{BT} = 820\ \mu$H

$C_g = 10$ pF
$C_A = 0.8$ pF
$C_{ISO} = .050$ pF

$f_{in} = 320$ MHz
$f_{out} = 4.0$ GHz
$g_m = 30\ \mu$S

$R_g = 6.5\ \Omega$
$R_A = 6.0\ \Omega$

Figure 3-12. Equivalent Circuit for Planar Triode.

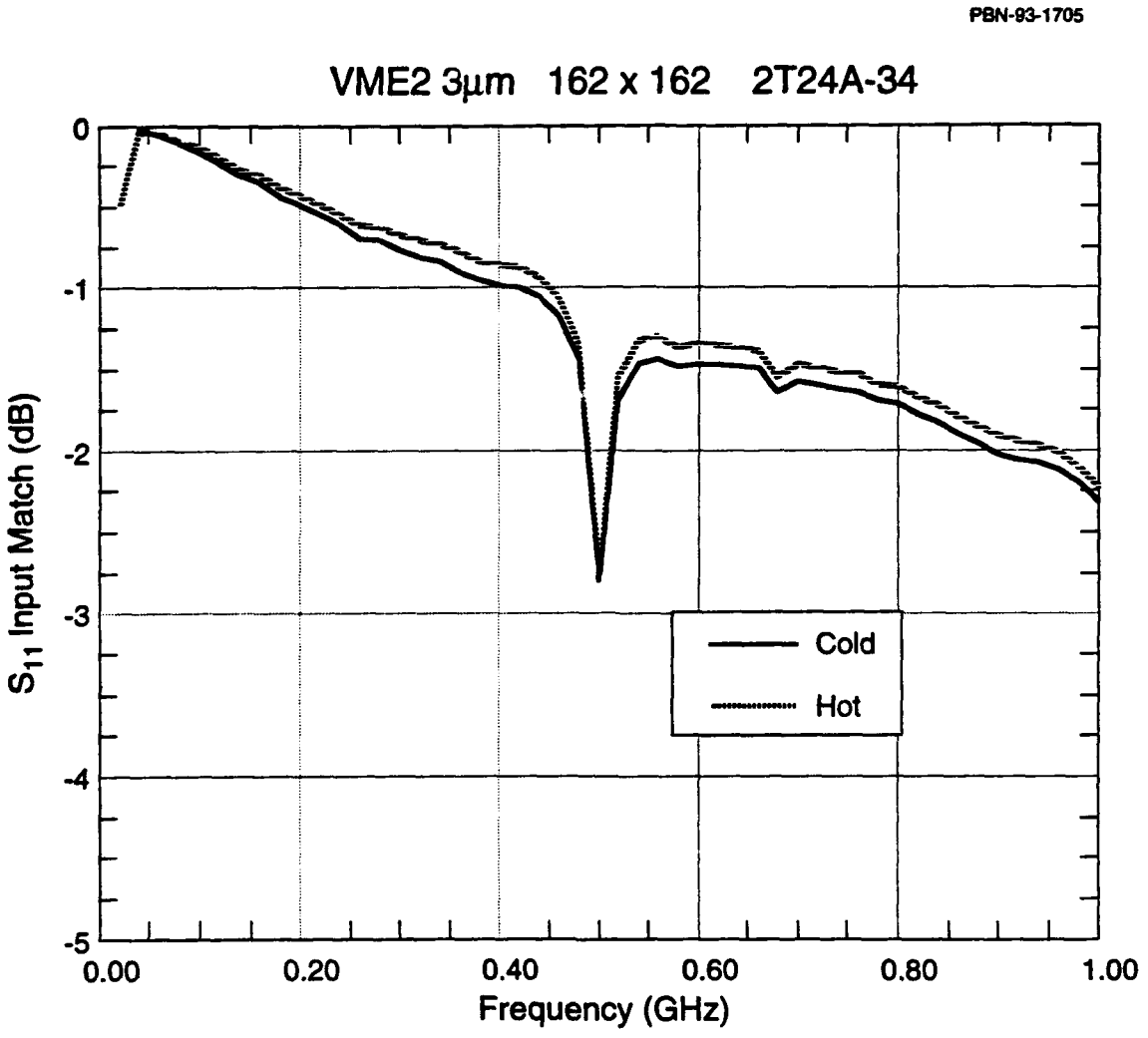


Figure 3-13. S_{11} Input Match for Planar Triode.

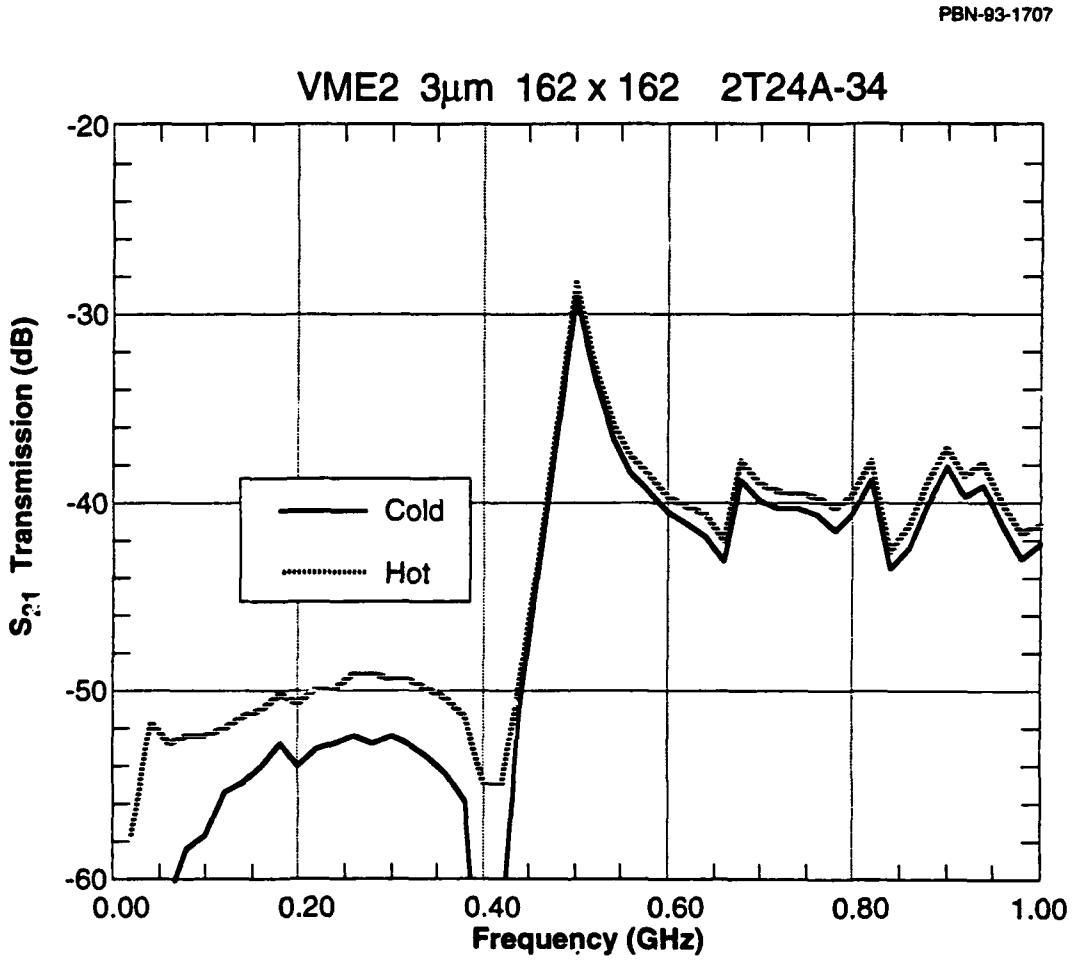


Figure 3-14. S_{21} Transmission for Planar Triode.

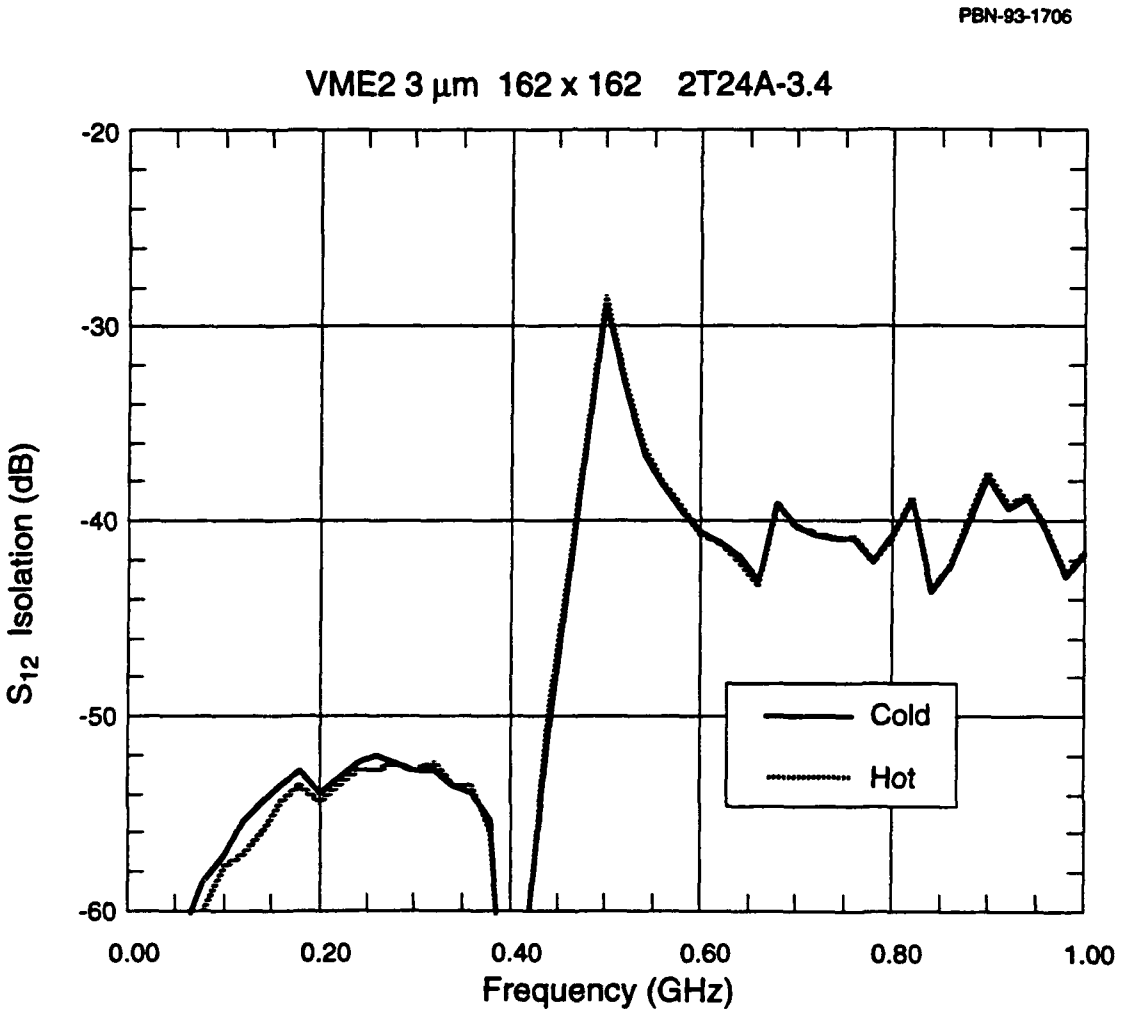


Figure 3-15. S_{12} Isolation for Planar Triode.

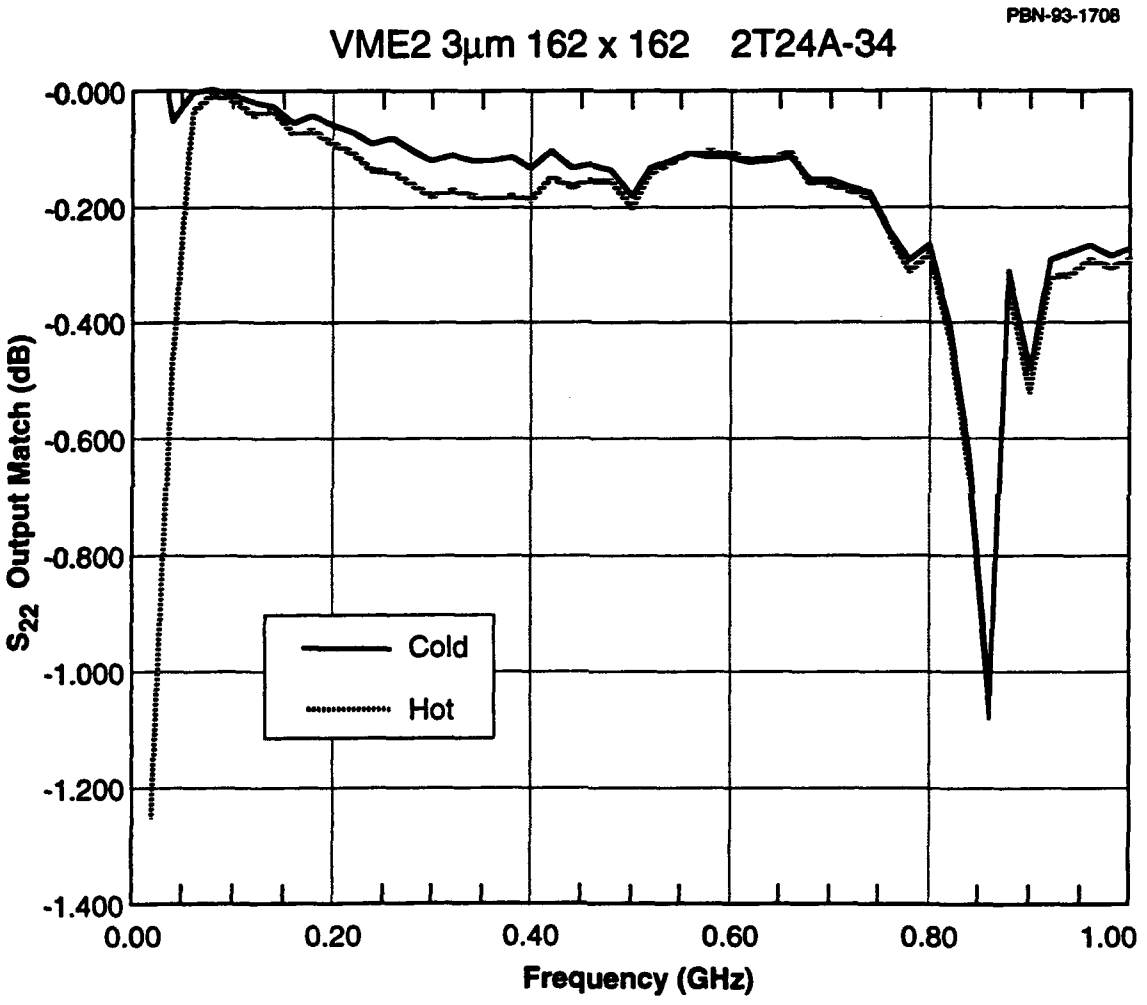


Figure 3-16. S_{22} Output Match for Planar Triode.

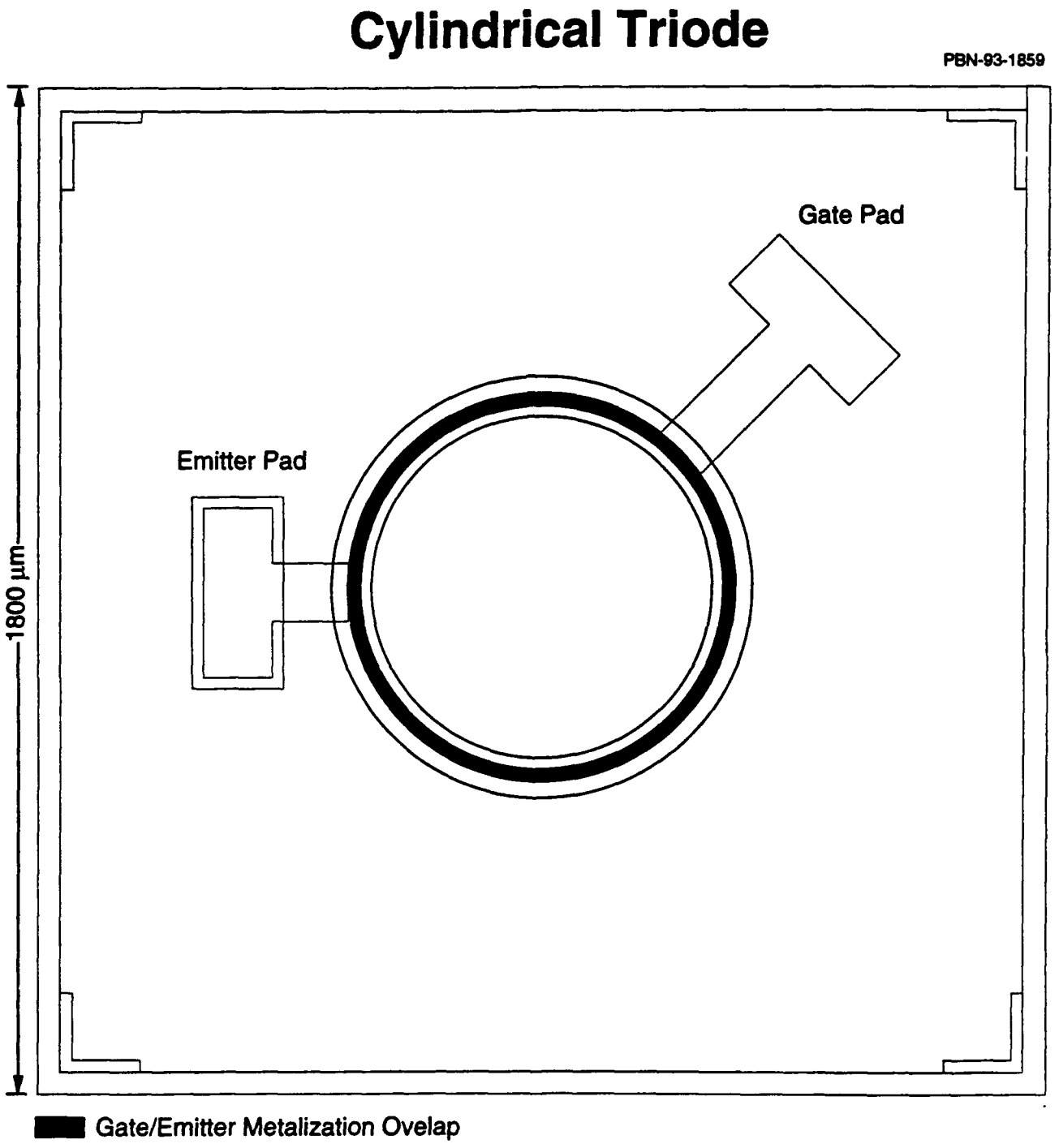


Figure 3-17. Layout of Cathode for Cylindrical Triode.

These chips were first tested in the chamber using the upper position in dc test alumina (Figure 3-4). Good chips were selected and sealed into a glass micro-triode. The equivalent circuit of this device is shown in Figure 3-18.

This device was biased with the gate at dc ground and the cathode pulsed negative with a half sine wave rectified 60 Hz signal (27% duty). The anode was held positive at 1,000 volts. The measured and extrapolated data from this device is shown in Figure 3-19.

The measured I/V data was fit to a Fowler-Nordheim curve to calculate the g_m (and therefore F_t) and allows extrapolation to higher gate voltages. The measured data yields an F_t of 100 MHz. Extrapolation to a gate voltage of 130 volts and a current of 60 milliamps yields an F_t of 1 GHz. This is equal to 2 micro-siemens per tip. Our best dc result (Figure 3-7) was 0.8 micro-siemens per tip. Therefore, this extrapolation is not too unreasonable. The glass package of this device was limited in bandwidth to about 100 MHz and therefore microwave tests were not performed.

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Equivalent Circuit for Cylindrical Trial Tests

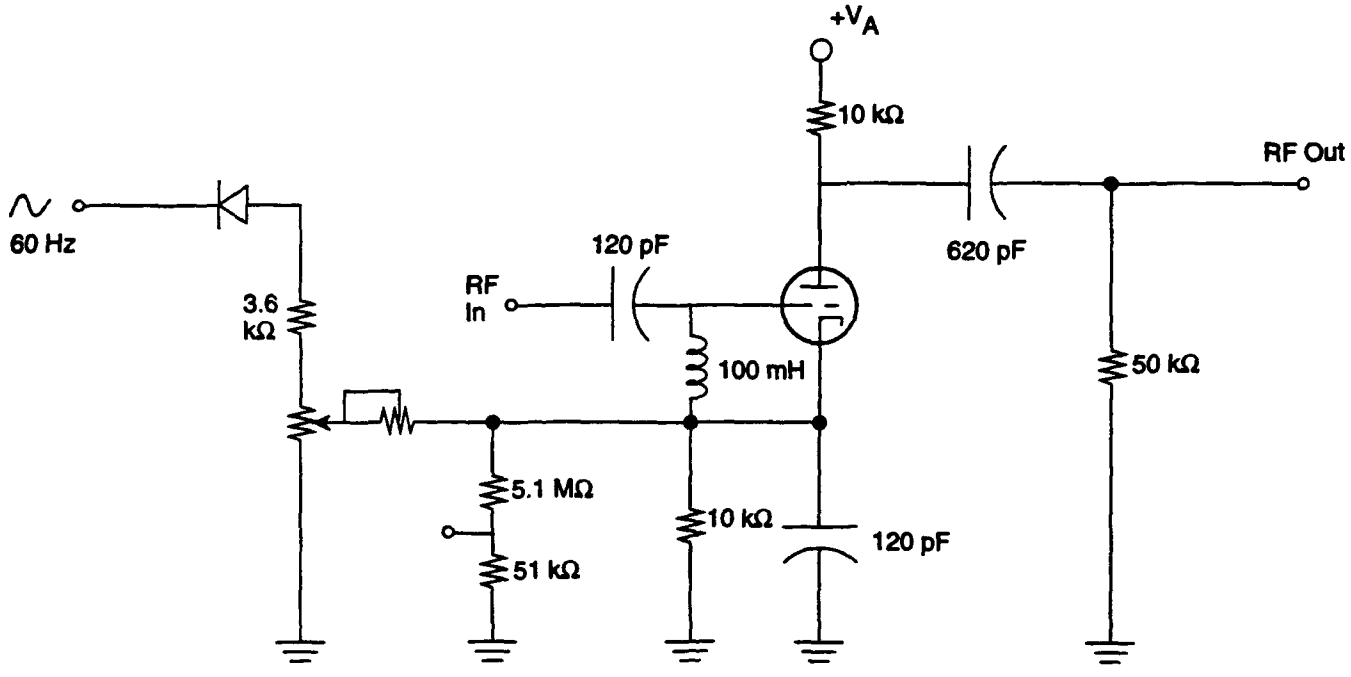

Figure 3-18. Equivalent Circuit for Cylindrical Triode.

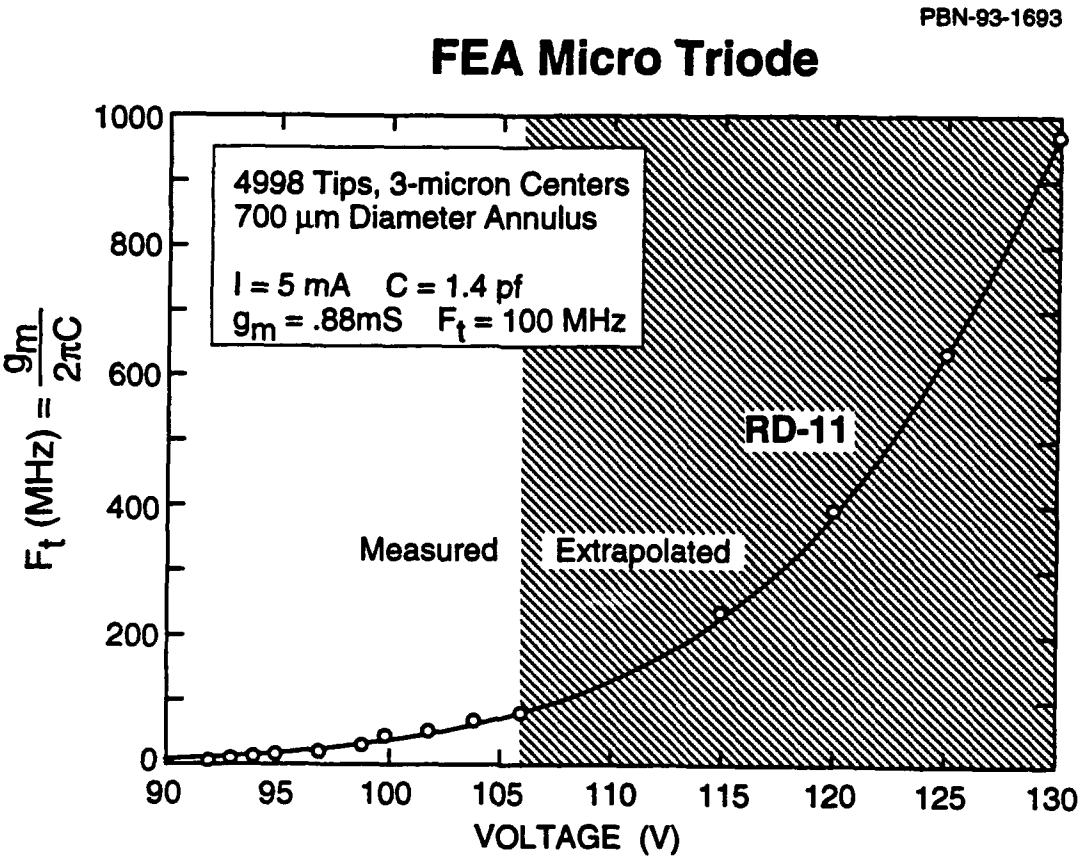

Figure 3-19. Measured and Extrapolated F_t for Cylindrical Triode.

4.0 CAPACITANCE MEASUREMENTS

It was realized after the first iteration was completed and tested that smaller devices were required to meet the F_t requirement. Maximum capacitances of less than 0.2 pF are probably required. To this end, a second design, layout and fabrication iteration was performed on the planar triode design. The second iteration planar cathode layout is shown in Figure 4-1.

As before, variety of structures were included to help characterize the capacitance. The top structure is a two-port that allows the cathode to be "tuned". All the other structures are one-port. The second structure from the top is a series of 20 edges each 120 microns long with 4 micron overlap of metalization (Figure 4-2). The third structure is and under-dense array of 20 rectangles each 17 by 25 microns (Figure 4-3). The bottom structure is a dense square 70 by 70 microns (Figure 4-4).

For each of the last three structures, there are four devices per chip. Two are connected to bonding pads, one is only RF probeable and the last is also RF probeable but does not have any tips. Also, along the bottom there is an RF probeable open, short, and large capacitor. Wafers were fabricated on two different substrates; sapphire and silicon, and with three different tip to tip spacings; 4, 3, and 2.5 μm. A table of the design parameters and predicted characteristics are shown in Figure 4-5.

For each structure, the three different hole pitches are listed. The value of **Area-1** is the area of where there is overlapped metal and is used to calculate the parallel plate capacitance. Given our target of 2 micro-siemens per tips, an F_t can be calculated. The value of **Area-2** is the total area for current density purposes and is used to calculate J at out target current of 20 micro-amp per tip.

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VMERF Number 2—Planar Triode

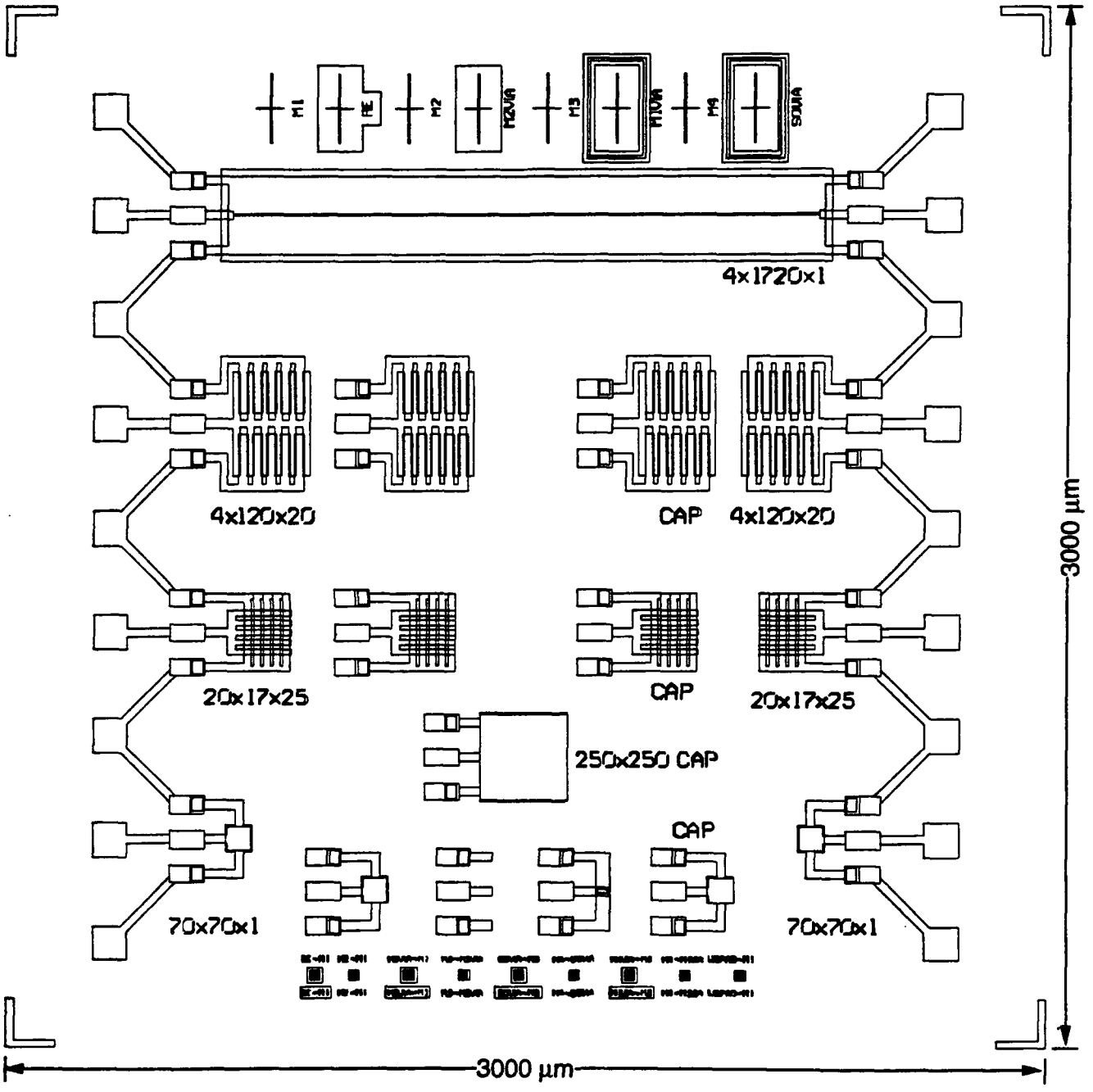

Figure 4-1. Layout of Second Iteration of Planar Triode Cathode Chip.

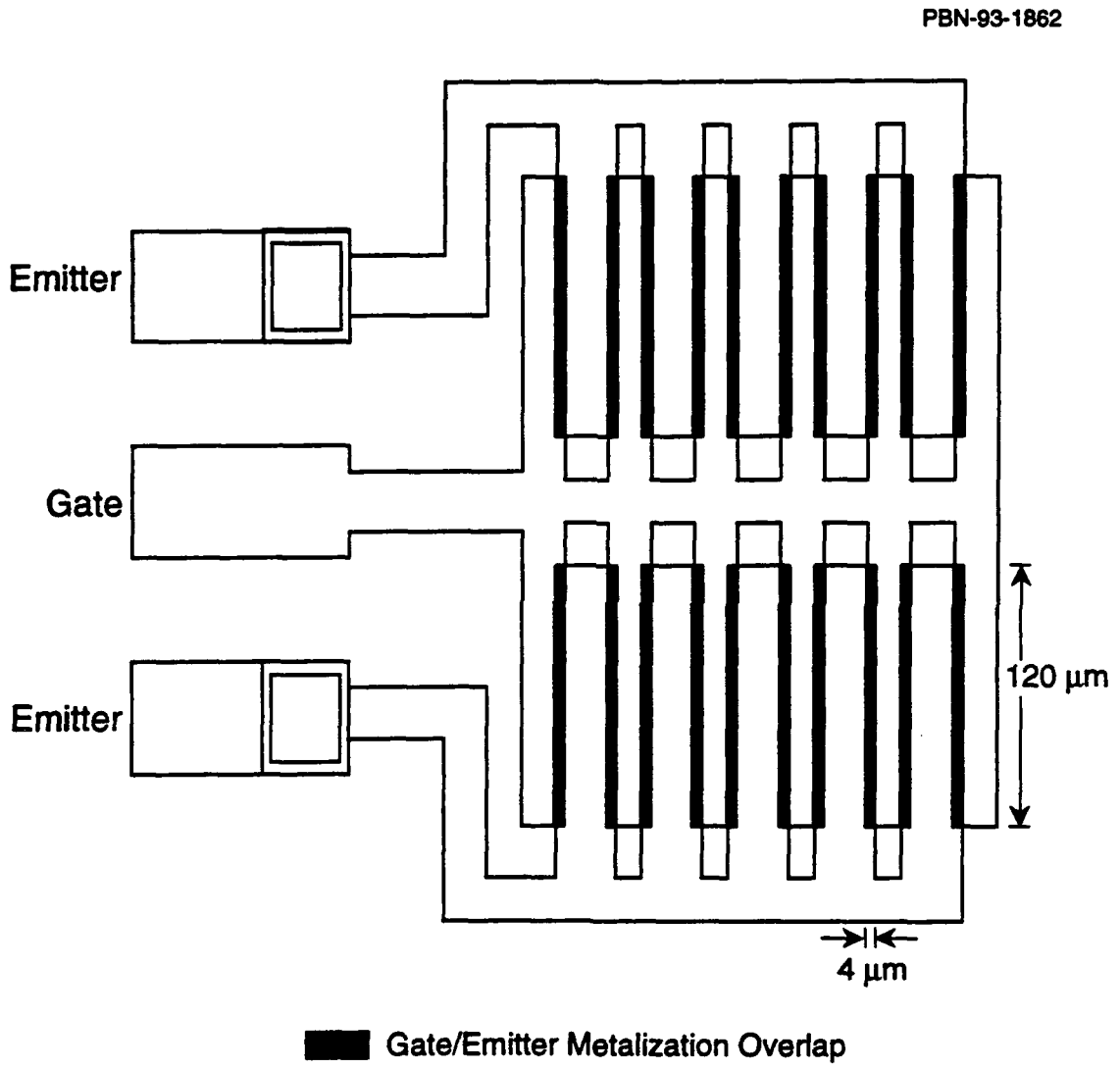

Figure 4-2. Enlargement of 20 Edges Structure.

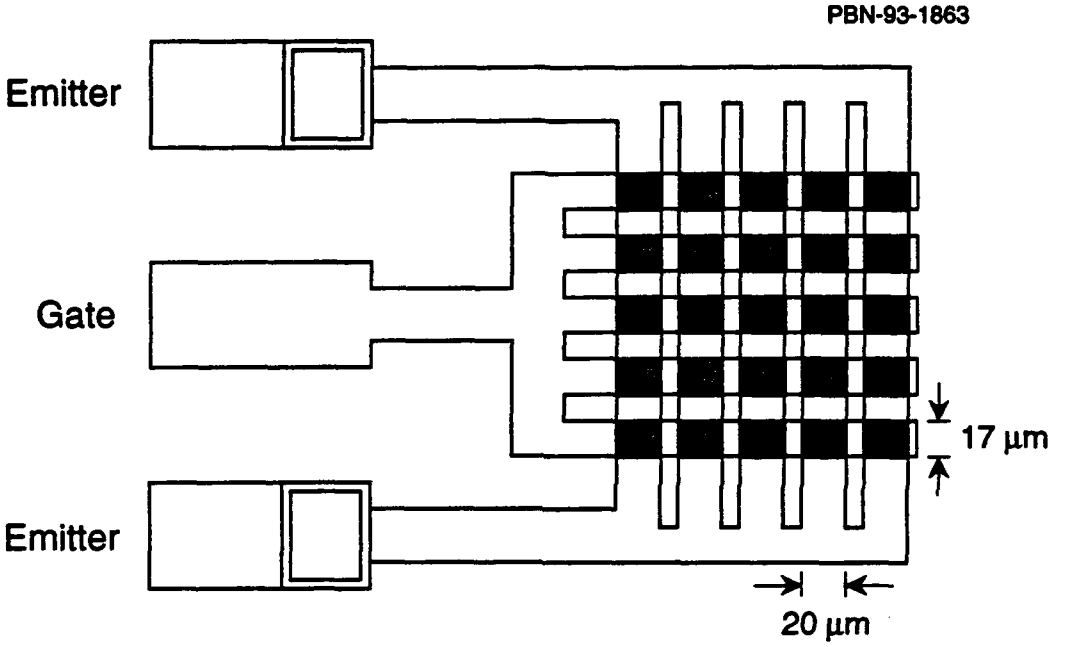

Figure 4-3. Enlargement of 25 Under Dense Structure.

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Dense Square Configuration

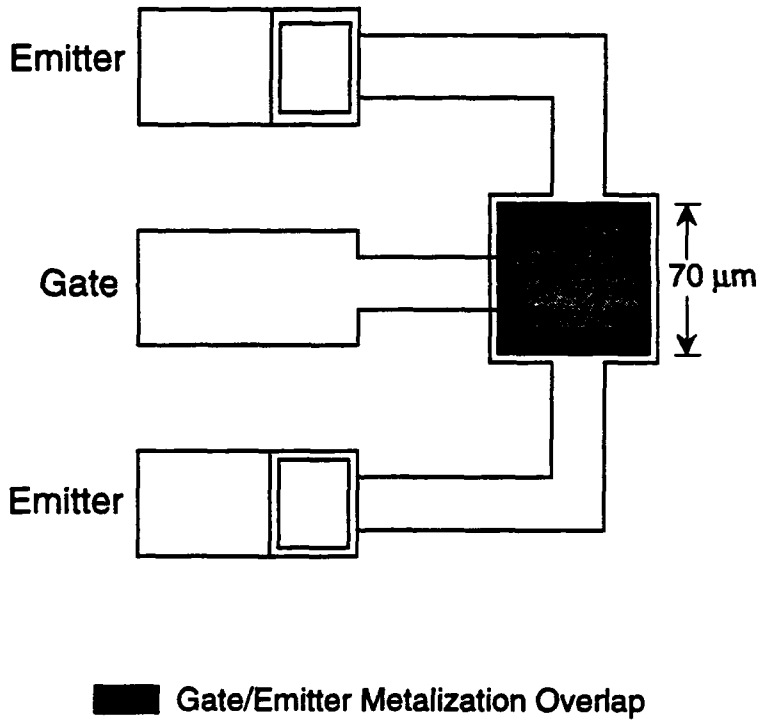

Figure 4-4. Enlargement of Dense Square Structure.

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Circuit	Size(μm)	Pitch (μm)	#/edge	Number total	Area-1 (μm^2)	C (pF) Parallel Plate 1 μm Dielectric	f_T (GHz) @2 μs/tip	Area-2 (cm^2)	J (I/cm^2) @20 μA/tip
line	4x1720x1	4.0	429	429	6880	.23	.59		
		3.0	572	72	6880	.23	.79		
		2.5	686	686	6880	.23	.95		
20 edge	4x120x20	4.0	29	580	9640	.32	.58	4.18e-4	28
		3.0	39	780	9640	.32	.78	4.18e-4	37
		2.5	47	940	9640	.32	.93	4.18e-4	45
25 sqr	20x17x25	4.0	3	225	8500	.28	.26	2.25e-4	20
		3.0	4	400	8500	.28	.45	2.25e-4	36
		2.5	5	625	8500	.28	.71	2.25e-4	56
Dense	70x70x1	4.0	16	256	4900	.16	.51	4.9e-5	104
		3.0	21	441	4900	.16	.88	4.9e-5	180
		2.5	26	676	4900	.16	1.3	4.9e-5	276

Figure 4-5. Design Parameters of Planar Triode Cathodes.

The structures were on chip RF probed with standard MMIC probes on a vector network analyzer. A TRL calibration was used on the network analyzer and verified to 15 GHz. The phase delay of S_{11} at 1 GHz was used to calculate the capacitance. The magnitude is a measure of the loss. There was a constant 6 ohm loss that was independent of frequency that is assumed to be contact resistance. At these frequencies it was not possible to see any loss due to metal resistance or dielectric. The total capacitance has been approximated as:

$$C_{tot} = K_{tips}(K_{layout} C_{||}) + C_{leads} + C_{pads}$$

where $C_{||} = \varepsilon_o A/d$ is the calculated parallel plate capacitance, C_{pads} is from the bonding pads, C_{leads} is from the leads and RF probeable pads, K_{layout} is for edge and other layout effects, and K_{tips} is due to the hole and tip. The measurement of the large capacitor is used to calculate "d". The relative dielectric constant for the SiO_2 is assumed to be 3.7. The difference between the devices with and without bonding pads is used to calculate C_{pads}. The dielectric thickness "d" was found to be 1 micron for the silicon wafer and 0.8 micron for the sapphire wafer. A best fit was made over many measurements and tabulated in Figures 4-6 and 4-7 for silicon and sapphire substrates respectively. The last two columns indicate how good the fit is to formula.

These results show some surprising effects. First, is the difference in the parasitic and edge effects between the sapphire and silicon. It appears that the bottom SiO_2 layer and the first level metal do not completely shield the substrate and therefore the substrate contributes to the stray capacitance. This effect is shown by the increased values of K_{layout}, C_{pads}, and C_{leads} of the silicon relative to the sapphire. The second effect that is unexpected is the difference due to the tip density. For the silicon, the tips cause an increase in capacitance with increasing density while for the sapphire, there is a decrease. An examination of a silicon wafer with holes and no tips did not show

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Silicon substrate			d=1 μm						
Device Type	Tip Pitch (μm)	$C_{\|\|}$ (pF) calc.	K_{layout} calc.	C_{device} (pF) calc.	K_{tips} calc.	C_{leads} (pF) meas.	C_{pads} (pF) meas.	C_{tot} (pF) calc.	C_{act} (pF) meas.
20 Edge	4	.32	2.0	.64	1.01	.10	.15	.90	.87
20 Edge	3	.32	2.0	.64	1.17	.10	.15	1.00	.99
20 Edge	2.5	.32	2.0	.64	2.86	.10	.15	2.08	-
25 sqr	4	.28	1.4	.39	1.01	.10	.15	.65	.63
25 sqr	3	.28	1.4	.39	1.17	.10	.15	.71	.67
25 sqr	2.5	.28	1.4	.39	2.86	.10	.15	1.37	1.08
Dense	4	.16	1.0	.32	1.01	.10	.15	.41	.41
Dense	3	.16	1.0	.32	1.17	.10	.15	.44	.44
Dense	2.5	.16	1.0	.32	2.86	.10	.15	.71	.89

Figure 4-6. Best Fit of Measured Data to Capacitance Model - Silicon.

PBN-93-1710a

Sapphire substrate			d = 0.8 μm						
Device Type	Tip Pitch (μm)	$C_{\|\|}$ (pF) calc.	K_{layout} calc.	C_{device} (pF) calc.	K_{tips} calc.	C_{leads} (pF) meas.	C_{pads} (pF) meas.	C_{tot} (pF) calc.	C_{act} (pF) meas.
20 Edge	4	.40	1.6	.64	.80	.03	.02	.56	.53
20 Edge	3	.40	1.6	.64	.61	.03	.02	.44	.47
20 Edge	2.5	.40	1.6	.64		.03	.02		
25 sqr	4	.35	1.2	.42	.80	.03	.02	.39	.42
25 sqr	3	.35	1.2	.42	.61	.03	.02	.32	.38
25 sqr	2.5	.35	1.2	.42		.03	.02		
Dense	4	.20	1.0	.20	.80	.03	.02	.21	.20
Dense	3	.20	1.0	.20	.61	.03	.02	.17	.15
Dense	2.5	.20	1.0	.20		.03	.02		

Figure 4-7. Best Fit of Measured Data to Capacitance Model - Sapphire.

this effect. There is no obvious reason why the substrate material would effect hole or tip capacitance since the bottom SiO_2 layer and the first layer of metal should serve as a ground plane. It might be that the process steps involved in making the tips has a side effect that is not understood relative to the silicon.

The sapphire results are quite encouraging. They show that true low capacitance structures are possible and are close to the parallel plate values. The dense arrays have capacitances under 0.2 pF. Another important conclusion from this capacitance study is that just using the parallel plate value can be quite inaccurate for certain geometries. For the sapphire substrate line emitters, the edge effects increased the capacitance by 60 percent while on silicon it was 100 percent. One design concept has been to make line arrays and then over-etch the dielectric to reduce the dielectric to that of vacuum. The problem as seen from the data is that most of the gain will be lost from increased edge effects. Also, on the silicon substrate the parasitic capacitances of the pads and leads were on the same order as the active area contribution for the small devices! The only safe approach for obtaining a true gate capacitance value (and therefore F_t) is to measure the actual capacitance at the operating frequency.

5.0 CONCLUSIONS

As shown in the body of this report, three of the four goals were met. The most difficult goal was F_t and our best results were an order of magnitude too low. To meet this goal both an increase in the transconductance g_m and a decrease in gate capacitance C_g are desired. For the Fowler-Nordheim emission that characterizes these cathodes, there are two ways to increase g_m. The first is to increase the current, since to first order g_m scales with current. The problem is that there is a current limit above which the cathodes self destruct and anode dissipation becomes a problem. The second approach is to decrease the gate voltage. This may be done in two ways; by reducing the gate to tip spacing or by reducing the work function at the tip surface. As demonstrated in Section 4.0, there is not much more that can be done about the capacitance issue for a simple triode amplifiers or the use of these emitters as gated cathodes for conventional tubes. The improvement must come in the g_m term for these applications. (There is a possibility of making a compact distributed type amplifier in which the capacitance can be overcome.)

Even with a device with a measured dc F_t at 1 GHz, it will be hard to get true power gain at frequency as a triode. As shown in Section 3.2.3, the input and output are highly mismatched. These triodes are relatively high impedance devices compared to the standard 50 ohm environment. The dc impedance which is an indicator of the RF impedance is just the inverse of g_m which for a target device is about 1000 ohms. The input must be transformed up and the output must be transformed down. However, operation at the high impedance will enhance the deleterious effect of the gate to anode capacitance. This impedance problem is not as bad for a gated cathode application as for triode operation.

The future work under the option portion of this contract will be towards increasing g_m. The total current may possibly be increased by improved process uniformity, improved cleaning procedures, and optimized turn on procedures. Modifications will be made in the process to try to decrease the tip to gate spacing. Finally, we will attempt to reduce the work function, and therefore, the operating gate voltage by applying coatings to the tips with a variety of materials with various deposition techniques. When improved cathodes are available, microwave testing will be performed to confirm the high frequency operation.